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European Patent Office  
Office européen des brevets

⑪ Publication number:

**O 135 864**  
**A2**

⑫

## EUROPEAN PATENT APPLICATION

⑬ Application number: 84110538.0

⑮ Int. Cl. 4: **G 11 C 29/00**

⑭ Date of filing: 05.09.84

⑯ Priority: 28.09.83 US 536597

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⑰ Date of publication of application: 03.04.85  
Bulletin 85/14

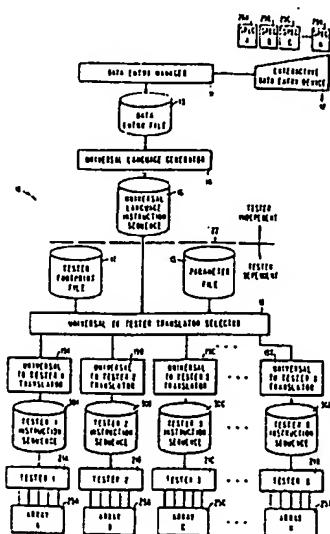
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⑳ Designated Contracting States: DE FR GB

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### ㉒ System and method for automatically testing integrated circuit memory arrays on different memory array testers.

㉓ A system for automatically testing a plurality of memory arrays (25A...25X) on selected memory array testers (21A...21X) includes an interactive data entry device (12) for entering array test specifications (20A...20N) including characterizing information, DC testing parameters, AC testing parameters and AC test pattern choices for the array. The test specifications are entered in a format which is independent of a particular tester's characteristics. A universal language generator (14) generates a tester independent universal language instruction sequence (16) for carrying out the prescribed tests based upon the entered test specifications. Associated with each tester is a language translator (19A...19X) which translates the tester independent universal language instruction sequence into an instruction sequence which is particular to the associated tester (21A...21X). The tester dependent instruction sequence (30A...30X) may be loaded into the associated tester to produce the test signals for testing the memory array (25A...25X).



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SYSTEM AND METHOD FOR AUTOMATICALLY TESTING INTEGRATED  
CIRCUIT MEMORY ARRAYS ON DIFFERENT MEMORY ARRAY TESTERS

This invention relates to the testing of integrated circuit memories and more particularly to a system and a method for automatically testing a memory array on a selected one of several different array testers.

5       Integrated circuit memory arrays are widely used for storing data in data processing systems. As is well known to those skilled in the art, an integrated circuit memory typically comprises a plurality of memory cells arranged in an array or matrix having a predetermined 10 number of rows and columns, with one data bit being stored per cell. Data is typically stored into or fetched from the array by addressing one or more cells and then reading or writing the desired data.

15       In the current state of the art, two hundred fifty-six thousand or more cells may be integrated on a single semiconductor substrate. Such arrays present extreme problems in the testing environment.

20       Among the tests typically performed on an array are DC parametric tests, AC parametric tests and AC pattern tests. DC parametric tests relate to static electrical properties such as voltage or current limits for the array cells and connecting lines. DC parametric tests may be performed on integrated circuits having interconnected memory cells thereon, (i.e., product tests) or on integrated circuits having unconnected devices thereon (i.e., test site tests). AC parametric tests relate to dynamic electrical properties such as minimum bit/word 25 address access time, and minimum cell switching trans-

ition times. AC pattern tests read and write various well known test patterns into the array to ensure that each cell is functioning properly and is not disturbed by operations performed on other cells. Examples of well 5 known AC pattern tests are walking 1's, marching 1's, or checkerboard pattern tests. Memory testers typically include a tester memory for storing therein an instruction sequence representing all of the tests to be performed on the array, and a tester pattern generator for 10 generating the appropriate address, control and data signals from the stored instruction sequence in the tester memory.

From the above description it will be appreciated that for a large array, generation of the requisite 15 tester memory instruction sequences is inordinately complex and time consuming. The instruction sequences for the tester memory must be created and debugged manually, a process that may take weeks when dealing with a two hundred fifty-six thousand bit array. Moreover, in 20 order to properly generate the instruction sequence, the test designer must be intimately familiar with the configuration of the tester being employed and the instruction set therefor. Further, an array manufacturing facility may often employ a number of different 25 memory testers each having different instruction sets. Memory test data must be created anew when another tester is employed, since there is usually no software compatibility even between different types of memory testers from the same manufacturer. Accordingly, additional 30 weeks of test generation and debugging may be required when it is desired to add or change testers array.

State of the art memory testers have attempted to alleviate some of the manual work of creating an appropriate tester instruction sequence by designing the 35 tester to accept a higher level instruction set.

However, such high level instructions are still tester dependent, i.e., they are particular to a given tester. Thus, the test designer must be intimately familiar with the high level instruction set for each tester 5 being employed. Moreover, the high level instruction sequence that defines the test program must be created anew when a different tester is employed. Accordingly, while the high level language provisions of state of the art memory testers have eliminated some of the more 10 tedious work, they have not solved the problems faced in a manufacturing environment which must test many array types on a plurality of different array testers.

It is therefore a primary object of the invention to provide a method and apparatus for automatically testing 15 integrated circuit memory arrays on a selected one of different memory array testers, so that the test designer need not know the hardware configuration or the instruction set employed by the tester.

It is a further object of the invention to provide 20 such a method and apparatus which are usable on any of a number of given memory testers, and which are expandable to new memory testers as they become available.

It is yet a further object of the invention to provide a method of generating instruction sequences for 25 a particular memory array in a particular tester in essentially reduced time.

The system and method of the invention for achieving these objects and other advantages are defined in the claims.

30 An array test system is disclosed which includes an interactive data entry device upon which menus are presented for entering test specifications which may in-

clude characterizing information, DC testing parameters, AC testing parameters, and/or AC test pattern choices for the array to be tested. The characterizing information, DC testing parameters, AC testing parameters and AC test 5 pattern choices are specified by the memory designer in an array test specification document and are entered into the interactive data entry device in a format which is independent of individual tester characteristics. Means are provided for automatically auditing the entered test 10 specifications, to ensure the consistency and completeness thereof.

The array test system disclosed also includes a universal language generator which generates tester independent instructions for carrying out the prescribed 15 DC parametric tests, AC parametric tests, and/or AC pattern tests based upon the test specifications which were entered into the interactive data entry device. The generated universal language instruction sequence is independent of the characteristics of an individual 20 memory tester. Finally, associated with each tester is a universal language translator which translates the tester independent, universal language instruction sequence into an instruction sequence which is particular to the associated tester, for carrying out the specified DC 25 parametric tests, AC parametric tests and/or AC pattern tests thereon. The universal language instruction sequence is routed to the translator associated with the tester to be employed, where the universal language instruction sequence is translated into the requisite 30 tester dependent instruction sequence. The translated tester dependent instructions are entered into the tester memory for producing the test signals which are used to test the array.

Since the disclosed apparatus which incorporates the 35 present invention automatically generates the instruction

sequences for testing a particular array on a given tester from a high level tester independent description, a set of memory test patterns may be generated in hours and not weeks. Moreover, the user need not understand 5 the hardware configuration or instruction set for the particular tester to be employed. Finally, an array can easily be tested on another tester by translating the universal language instruction sequence for the array using the universal language translator associated with 10 another tester. When new testers become available, a new translator merely need be made therefor in order to integrate that memory tester into the automatic memory test signal generating system.

In a preferred embodiment, the interactive data 15 entry device is a display terminal, e.g., an IBM 3277, upon which appear menus for prompted entry of characterizing information, DC testing parameters, AC testing parameters and AC test pattern choices for the particular array. A data entry manager within a host data processor, e.g., an IBM 3033 controls the interactive data 20 entry. The universal language generator may reside in the same host processor, for generating the tester independent instruction sequence from the interactively entered tester independent information and parameters. 25 The translators each may reside in the same host data processor or another data processor, for translating the universal language instruction sequence into an appropriate tester dependent instruction sequence.

The method of testing arrays according to the 30 present invention is particularly suited to include the steps of

(a) presenting menus on an interactive data entry device for entry therein of characterizing information, DC testing parameters, AC testing parameters and AC test 35 pattern choices for the array to be tested; and

(b) verifying the accuracy and completeness of the entered information, and alerting the operator of any incomplete/inaccurate information; prior to generating a universal, tester independent instruction sequence based 5 upon the entered information and then translating the universal language instruction sequence into a tester dependent instruction sequence for the particular array tester to be employed.

10 In the following, an embodiment of the invention is described with reference to the drawings listed below:

Fig. 1 illustrates the overall architecture of a system for automatically testing selected memory arrays on selected memory array testers according to the present invention.

15 Fig. 2 illustrates the data entry manager employed in the system of Fig. 1.

Fig. 3 illustrates sample interactive display screens for entering therein array characterizing information, DC testing parameters, AC testing parameters and 20 AC test pattern choices.

Fig. 4 illustrates the screen image manager and auditor employed in the data entry manager of Fig. 2.

Fig. 5 illustrates the universal language generator employed in the system of Fig. 1.

25 Fig. 6 illustrates the DC universal language generator employed in the generator of Fig. 5.

Fig. 7 illustrates the AC universal language generator employed in the generator of Fig. 5.

30 Fig. 8 illustrates a universal to tester translator which may be employed in the system of Fig. 1.

Fig. 9 illustrates a typical array tester which may be employed in the system of Fig. 1.

Fig. 10 illustrates bit pattern generation data employed by the translator of Fig. 8.

Fig. 11 illustrates a typical checkerboard bit pattern generated by the translator of Fig. 8.

Overall System Architecture and Operating Principles

Referring now to Fig. 1, there is illustrated the 5 overall system architecture and methodology for automatically testing a plurality of memory arrays on selected memory array testers. The system 10 includes an interactive data entry device 12 for entering therein array test specifications, which may include characterizing information, DC testing parameters, AC testing parameters and/or AC test pattern choices for the particular memory array 25A...25X to be tested. This information may be found in the memory test specification 10 document 20A...20N for the array to be tested.

15 Data entry manager program 11 resides in a host computer to which interactive data entry device 12 is connected. Data entry manager 11 is employed for presenting menus on interactive data entry device 12 and for placing data entered thereby into data entry file 13. 20 The data in entry file 13 characterizes the memory and the tests to be performed thereon and is independent of any particular tester configuration. The data from entry file 13 is configured into a universal, tester independent language sequence 16 by universal language generator 25 14.

The universal language sequence 16 is then applied to the appropriate one of the plurality of universal to tester translators 19A...19X one of which exists for each tester 21A...21X which is employed for testing an array 30 25A...25X thereon. Universal to tester translator selector 18 applies the universal language sequence 16 to the appropriate translator 19A...19X in accordance with tester routing data contained in parameter file 15. Each

universal to tester translator 19A...19X can translate the tester independent universal language sequence 16 into a tester dependent instruction sequence 30A...30X. The tester instruction sequences 30A...30X are applied to 5 the tester memory of associated tester 21A...21X. The tester instruction sequences are used by the tester pattern generator to generate the test signals for carrying out the appropriate DC parametric, AC parametric and AC pattern tests.

10 Examination of Fig. 1 shows that any one of arrays A...N may be tested on any one of testers 1...X without the need for regenerating the test data. Rather, the universal language instruction sequence is merely applied to the appropriate universal to tester translator 19 for 15 generating the appropriate tester instruction sequence 30. Moreover, since all of the processing above line 22 is tester independent, the user at interactive data entry device 12 need not know anything about a particular tester configuration or instruction set. He need merely 20 enter the appropriate data from the memory test specification 20 into interactive data entry device 12 as prompted by data entry manager 11. Finally, a new tester may be added by generating a new universal to tester translator 19 for interfacing the added tester with the universal 25 language instruction sequence.

Fig. 1 also outlines the method of automatically testing the selected memory array 25 on a selected tester 21. The memory characterizing and test data is entered via interactive data entry device 12 and a universal 30 language representation thereof is generated by universal language generator 14. The universal language instruction sequence is then applied to the appropriate universal to tester translator 19 by universal to tester translator selector 18. The tester instruction sequence 35 produced by the appropriate translator is then stored in

the tester memory and used to generate the test signals for testing array 25.

In succeeding sections of this specification, each of the components of Fig. 1 will be described in sufficient detail so as to enable those skilled in the art to make and use automatic memory test system 10.

#### Interactive Data Entry

Referring now to Fig. 2, the details of data entry manager 11 will be described. Data entry manager 11 creates a data entry file 13 from data which is interactively entered by the user at interactive data entry device 12. As noted above, interactive data entry device 12 is a display terminal, e.g., an IBM 3277, which is connected to a host computer, e.g., an IBM 3033. A user interactively enters memory test data from the memory test specification 20 in a manner that will be illustrated in connection with Figs. 3A-3L.

Referring again to Fig. 2, data entry manager 11 includes a screen image manager and auditor program 26 for controlling the data entry process by presenting the user with an appropriate display screen in a predetermined sequence to facilitate the interactive entry of characterizing information, DC testing parameters, AC testing parameters and AC test pattern choices for the particular array to be tested.

Screen image manager and auditor 26 employs two data bases in connection with this operation, i.e., skeleton data entry screens file 23 and error message file 24. Skeleton data entry screens file 23 is a representation of all of the screens which the screen image manager and auditor may present to a user. Some of the screens are pre-initialized to facilitate data entry as will be described in connection with Figs. 3A-3L. Figs. 3A-3L illustrate all of the skeleton screens employed. Each of

these screens and the fields contained therein will be described more particularly below.

A second function performed by the screen image manager and auditor 26 is auditing the interactively 5 entered data for possible errors. These audits may be generally described as syntax audits and test specification audits.

Error message file 24 contains informational 10 messages and audit error messages which may be presented to the user. If in auditing an error is detected, an appropriate error message from the error message data base 24 will be dynamically flashed onto interactive data entry device 12. Table 1 contains a listing of error 15 warning and informational messages employed, and a brief explanation of the meanings thereof. Output messages 27 are merely a hard copy of the error messages which are presented on interactive data device 12 during interactive data entry.

Table 1

ERROR WARNING AND INFORMATIONAL MESSAGES

ERROR 1: Product masterslice number must be 3 numeric digits.

5 Meaning: Self-explanatory.

ERROR 2: Product type is not "WAFER" or "MODULE" or "TEST SITE".

Meaning: 1 of the 3 above choices must be selected.

ERROR 3: Product footprint is not 11x11 or 17x17.

10 Meaning: The only allowable pin grids programmed into the system are 11x11 and 17x17.

ERROR 4: Tester \_\_\_\_\_ is not supported.

Meaning: The current list of allowable testers are:

\_\_\_\_\_, \_\_\_\_\_.

15 ERROR 5: Invalid "PART # ID".

Meaning: Self-explanatory.

ERROR 6: Disposition must be "NEW" or "MOD" or "DEL"

Meaning: Enter "NEW" if this is first session for this product and tester.

20 Enter "MOD" if AC or DC data has already been entered and you want to concatenate the complementary data to it.

Enter "DEL" to delete any existing data for this product and tester.

25 ERROR 7: Test Name \_\_\_\_\_ is not known to the directory of tests.

Meaning: Enter correct test site test name or update the directory of valid tests.

ERROR 8: Delay value for Test Number    does not have unit-of-measure specified.

Meaning: Specify either "MS" or "US" or "NS".

5           WARNING: Test number    Range between MAX LIMIT value and MIN LIMIT value is greater than .5 volts/amp.

Meaning: Insure pos/neg signs are consistent, and that values are correctly specified.

10           WARNING: Test Name    Unit-of-measure are unequal between MAX LIMIT value and MIN LIMIT value.

Meaning: Insure unit of measure denominations are correctly specified.

15           ERROR 9: Test Name    MAX LIMIT and MIN values are reversed.

Meaning: MAX LIMIT value is less than MIN LIMIT value.

ERROR 10: Power supply "CASE #" or "NUMBER OF CASES" is not numeric.

Meaning: Value must be 2-digit numeric.

20           ERROR 11: Power Supply Case #    IOCLAMP value incorrectly specified.

Meaning: Must be numeric value followed by: V or MV.

ERROR 12: Power Supply Case #    IORANGE value is not legal.

Meaning: Value must be selected from list provided.

25           INFO 1: Universal Language Controller began operation.

Meaning: Self-explanatory.

INFO 2: DC Universal Language Generator began operation.

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Meaning: Self-explanatory.

INFO 3: DC Universal Language Generator completed  
successfully.

Meaning: Self-explanatory.

The error and warning messages of Table 1 are employed by screen image manager and auditor 26 to audit the interactively entered data for completeness and consistency. ERROR 2 (Table 1) is an example of 5 syntax error, which occurs when incorrect "PRODUCT TYPE" information is entered on the DC Array Library Allocation Screen (Fig. 3B). When ERROR 2 message flashes on the screen the user is required to re-enter the erroneous data. ERROR 10 (Table 1) exemplifies a 10 specification error, which occurs when an unrecognized test site "TEST NAME" is entered on the DC Test Site Limits Menu Screen (Fig. 3G). An unrecognized test site "TEST NAME" may occur if the name was entered 15 incorrectly (e.g., misspelled) or if the directory of test site tests needs to be updated so that the test may be recognized.

The array test data which is interactively entered under the control of screen image manager and auditor 26 is placed in data entry file 13. Data entry file 13 20 is a partitioned data set containing the interactively entered data organized as a collection of filled in skeleton screens.

Referring now to Fig. 4, there is illustrated the 25 detailed architecture of screen image manager and auditor 26. Option menu processor 29 is the main controlling software. Option menu processor 29 deciphers the user responses to the presented screens (to be described in connections with Figs. 3A-3L) and determines which screens to display on interactive data entry device 12. Option menu processor 29 also determines which programs to call to process the interactively entered data. Finally, option menu processor 29 30 monitors activity within the other programs via return codes and provides a linkage with the skeleton data entry screen file 23 and error message file 24.

Allocation routine 32 processes the user's response to the AC and DC Allocation Screens (to be

described below in connection with Figs. 3B and 3C). The data entered in connection therewith is used to construct unique data sets in data entry file 13 for supporting subsequent processing.

5 DC test condition routine 31 processes the user data entered in connection with the Power Supply Screen, DC Test Limits Screen and DC Test Site Limit Screen (to be described more particularly in connection with Fig. 3E, 3F and 3G, respectively). Each of the 10 fields completed by the user is checked for proper syntax, completeness, and where possible for technical accuracy as will be described below.

15 AC test condition routine 33 processes the user information entered in connection with the Power Supply Screen and AC Array Test Limit Screen and Additional Pass Screen (to be described below in connection with Figs 3E, 3I, and 3J respectively). Each of the fields completed by the user is checked for proper syntax, completeness and where possible for technical accuracy 20 as will be described below.

25 System execution routine 34 interprets user responses on the Background Processing Menu (to be described in connection with Fig. 3L). System execution routine 34 sets up the required job control language for executing the requested user option as will be described below.

30 Referring now to Fig. 3, the interactive data entry screens presented on interactive data entry device 12 by data entry manager 11 will now be described. In connection with this description, the sequence of displaying the screens will be described along with the format and data entered therein. For ease of description, the entry of specific test data will be illustrated in connection with Fig. 3.

35 The data entered by the user is contained in a high level array test specification 20 which uniquely specifies the requisite DC parametric tests, AC

parametric tests and AC pattern tests which the array designer wishes to perform for the particular array. The information in high level specification 20 is tester independent, i.e., it specifies the requisite tests to be performed on the array without regard to the particular tester which will be employed..

When the system of the present invention is initialized, the Primary Option Menu Screen illustrated in Fig. 3A appears on the data entry device 12. This screen requires the user to select one of six options. Option 1 will cause the DC Array Library Allocation Screen of Fig. 3B to appear. Option 2 will cause the AC Array Library Allocation Screen of Fig. 3C to appear. Option 3 will cause the DC Test Screens illustrated in Figs. 3D-3G to appear in a sequence which will be described more particularly below. Option 4 will cause AC Test Screens illustrated in Figs. 3H-3J to appear in a sequence described below. Option 5 will cause the Foreground Processing Screen of Fig. 3K to appear while Option 6 will cause the Background Processing Screen of Fig. 3L to appear.

It will be noted that Options 1 and 2 must be selected prior to selecting Options 3 and 4, respectively. If this is not done, an appropriate error message will be displayed.

The interactive data entry screens of Figs. 3B-3C will now be described in detail. In order to more easily describe interactive entry of an array test specification, representative examples for both DC and AC tests will be illustrated from the user's view.

DC PRODUCT TEST EXAMPLE: For DC tests, both a DC product test (performed on an integrated circuit array of interconnected memory cells) and a DC test site test (performed on an integrated circuit chip having unconnected devices thereon) will be illustrated. The examples of the DC product test, DC test site test and AC test which are initially presented here, will be

carried through the remainder of this specification in order to illustrate how representative test data is processed through the entire test system of Fig. 1. For purposes of illustrating DC product test data

5 entry, assume that high level test specification 20 calls for an input current measurement on array pin P1, with the  $V_{CC}$  power supply being set to 2v and the  $V_{BB}$  supply being set to 0v. The test also requires a 200mV voltage to be applied to pin P1 while an 800mV voltage

10 is applied to pins P2 and P3. The measured input current should be between 100 and 500 $\mu$ A.

The above DC test data is entered as follows: When the Primary Option Menu screen of Fig. 3A appears, the user selects Option 1. This causes the DC Array

15 Library Allocation screen of Fig. 3B to appear. The Allocation Screen of Fig. 3B requires the user to enter a series of general product description parameters which will subsequently be used by the test system to uniquely allocate all the required data sets for

20 subsequent processing of DC test data. More particularly, referring to Fig. 3B, the "TECHNOLOGY" field identifies which array product family that is being tested. The "PRODUCT TYPE" field identifies the package level. The "PART # ID" and "ENGINEERING CHANGE

25 LEVEL" fields identify the specific array component within the array product family and its current design level. Finally, the "DISPOSITION" field identifies whether this session is generating a totally new set of DC test data or modifying existing data.

30 Upon completion of data entry in the Allocation Screen of Fig. 3B, screen image manager 26 will again present the Primary Option Menu of Fig. 3A. Then, in order to enter the DC Product test data of the above example, the user selects "DC TEST DATA ENTRY" (Option

35 3). Selection of Option 3 causes DC Test Data Entry Screen of Fig. 3D to appear. The DC Test Data Entry Screen allows the user to select the desired type of DC

testing information to be entered. The user enters a "PROJECT IDENTIFICATION" along with a "TEST PROGRAM" name whose format definition is described on the screen. The "MEMBER" field identifies which type of DC test data is to be accessed and updated. The format of the member field is the following:

5 "D"  
10      xxx -- technology  
      y - First letter of product type  
      z - Suffix level  
      "L" or "S" - "L" + test limits, S + supply.

15 After completing the DC test data entry screen of Fig. 3D, if selected, a selection list is provided to the user containing the available members according to the above described format for "MEMBER" field. In order to input the test data example described above, the user would select the power supply limits, and the Supply Menu Screen of Fig. 3E would appear.

20 Referring to Fig. 3E, the "POWER SUPPLY CASE NUMBER" field identifies each unique power supply configuration desired for testing. This allows the flexibility of different power supply configurations within the same DC array tests. The "POWER SUPPLY CASE NUMBER" field provides a link between the information 25 in the Supply Menu Screen of Fig. 3E and the Test Limit Screen of 3F as will be described below. This field is set to "1". The "TOTAL NUMBER OF CASES" field is merely the total number of unique power supply configurations which are defined by high level test specification 30. In this example, this field is set to "1". In order to enter the data of the above example, the user fills in the "V<sub>CC</sub>" fields for groups 1 and 2 with the keyword "V<sub>CC</sub>" and the "V<sub>BB</sub>" fields for groups 1 and 2 with keyword "V<sub>BB</sub>". By representing the power 35 supplies as two groups of power pins there is the flexibility of sharing physical power supply pins if product demands additional power pins for a given

supply voltage. This will be used in conjunction with the "MODE" field described below.

5 The "POWER SUPPLY CLAMP" voltage and compliance current "RANGE" values are preinitialized to standard values as shown in Fig. 3E. The user has the option of using the pre-initialized values or changing them. The "MODE" field can be one of three values for any one of the five power supplies  $V_{CC}$ ,  $V_{BB}$ ,  $V_{EE}$ ,  $V_{11}$ ,  $V_{22}$ .

10 The "STANDARD" mode is used when the number of power supply pins required for a given supply voltage for a given array product conform to the total number of supply pins available in groups 1 and 2. The "MULTIPLE" mode and "DUAL" mode are used when more than the total number of supply pins are needed than available in groups 1 and 2. "MULTIPLE" is used when a group 1 and/or group 2 is needed to be shared by only one supply setting. If group 1 and group 2 are needed to be shared by two different supply settings then "DUAL" will be used. The pre-initialized value is 15 "STANDARD". The "IOCLAMP" and "IORANGE" fields are pre-initialized to the values as shown in Fig. 3E. The user has the option of using the pre-initialized values or changing them.

20

25 Upon completing the Supply Menu Screen (Fig. 3E), the user again will be presented with the Data Entry Selection List as previously described. The user then selects the DC Test Limits Screen and the screen shown in Fig. 3F will appear. In order to supply the data for Fig. 3F the user first supplies an 8 character "TEST 30 NAME" which will be used to identify the test being specified. The "DIAGNOSTIC NUMBER" is pre-initialized to 1. The "DIAGNOSTIC NUMBER" will be used for failure correlation and the user can modify this number. The "DELAY" field allows the user flexibility to override 35 the system calculated delay. Otherwise, the system calculates a settling time delay for delaying the measurement time until the power supplies settle down.

In order to enter the data of the above described DC product test example, "P1", "500 $\mu$ A" and "100 $\mu$ A" are entered into the "MEASURED PIN", "HIGH LIMIT", and "LOW LIMIT" fields, respectively. The "POWER SUPPLY CASE NUMBER" field is set to "1" indicating which of the configurations in the power supply screen of Fig. 3E is to be used for this test. The "PIN" and "VALUE" fields of Fig. 3F contain any applied conditions required. In the particular example above, the following pins and values would be entered:

	<u>"PIN"</u>	<u>"VALUE"</u>
	P1	200mV
	P2	800mV
	P3	800mV
15	VCC	2V
	VBB	0V

The fields on the bottom third of Fig. 3F relate to the requirement of writing a pulse during the performance of a DC test. If high level test specification 20 calls for pulse writing, then the pulse is specified by filling in the bottom third of Fig. 3F. The "TYPE" field determines whether AC or DC switches are to be used. The "PIN" field is the pin number to be pulsed. The "LEAD" and "TRAIL" field define the leading and trailing edges of the pulse, entered as time value and units (e.g., 20ns for twenty nanoseconds). The return to zero field determines if it is a transition or complete pulse.

After DC Test Limit Screen of Fig. 3F is completed, the screen entry for a single DC product test is complete and the Primary Option Menu of Fig. 3A would again be displayed. Of course, a number of DC products test cases may be entered in the manner specified above.

35 In order to complete the description of interactive entry of DC test data, a second example will be illustrate entry of DC test site data.

DC TEST SITE TEST EXAMPLE: Assume that high level test specification 20 calls for a  $V_{BE}$  transistor measurement of between -500mv and -700mv. In order to enter this data, the above described interactive data entry 5 process would be followed except that the user would be presented with the DC Test Site Limit Menu of Fig. 3G, instead of the DC Test Limits Menu of Fig. 3F. Presentation of screen 3G as opposed to 3F would be determined by the data entered into the "PRODUCT TYPE" field 10 of the DC Array Library Allocation Screen of Fig. 3B.

Upon presentation of the DC Test Site Limits Menu of Fig. 3G, the user would enter a test name to identify the test being specified. The "PIN (POS)" and "PIN (NEG)" fields are employed to select what points on the 15 transistor are to be measured between. In the above example, only the positive pin needs to be specified and the user would input product pin corresponding to the emitter pin number. For illustration this is product pin P1. The value -500mV and -700mV are 20 entered into the "MAX LIMIT" and "MIN LIMIT" fields, respectively.

The "DIAGNOSTIC NUMBER" field is pre-initialized to "01". This field is used for failure correlation and can be modified by the user. The "POWER SUPPLY 25 CASE NUMBER" field is set to "1", thus indicating which of the configurations in the Supply Menu (Fig. 3E) is to be used. The "EMITTER PIN" and "EMITTER VALUE" fields are set to the emitter pin name (P1) and the applied current value (-10 $\mu$ A) as specified in high 30 level test spec 20. The "BASE PIN" (P2) is set to ground ("GND"). Likewise, the "COLLECTOR PIN" (P3) is set to ("GND"). Other conditions or process parameters may also be specified if required by high level test specification 20. Upon completion of the DC test site 35 tests, the user would return to the Primary Option Menu of Fig. 3A.

In order to complete the description of data entry screens of Fig. 3A-3L, an AC test example will be illustrated.

5 AC TEST EXAMPLE: The particular example illustrated will be a well known checkerboard test, incrementing in the word direction. The test is to be performed with a 100ns cycle time. The read and write pulses are 20ns and power supply Vcc is 0v, power supply Vbb is -2v and supply V<sub>EE</sub> is -5v.

10 As with the DC tests described above, the user begins with the Primary Option Menu Screen of Fig. 3A and selects option 2. The AC Array Library Allocations Screen of Fig. 3C will appear. The Allocation Screen of Fig. 3C requires the user to enter a series of 15 general production description parameters which will subsequently be used by the test system to uniquely allocate all the required data sets for subsequent processing of AC test data. More particularly, referring to Fig. 3C, the "TECHNOLOGY" field identifies 20 which array product family is being tested. The "PRODUCT TYPE" field depicts the package level. The "PART NUMBER" and "ENGINEERING CHANGE LEVEL" fields identify the specific array components within the general array product family and its current design 25 level. The "NUMBER OF WORD ADDRESSES" and the "NUMBER OF BIT ADDRESSES" define the address dimension of the array. The "NUMBER OF DATA LINES" define the data-in and data-out ports of the array. The "NUMBER OF CONTROL LINES" define the number of control gates 30 associated with the write, read or data line. The "DESIGN" field refers to the physical layout of the array, i.e., interwoven or non-interwoven. Finally, the "DISPOSITION" field identifies whether the session 35 is generating a totally new set of AC test data or merely modifying existing data.

Upon completion of data entry in the AC Array Library Allocations Screen of Fig. 3C, screen image

manager 26 will again present the Primary Option Menu of Fig. 3A. Then, in order to enter the AC test data of the above example, the user selects "AC TEST DATA ENTRY" (Option 4). Selection of Option 4 causes the AC 5 Test Data Entry Screen of Fig. 3H to appear. This screen allows the user to select the desired type of AC testing information to be entered. The information specified here has already been described above in connection with Fig. 3D.

10 After completing the AC Test Data Entry Screen of Fig. 3H, if selected, a selection list is provided to the user (as was described above) which allows a choice of either power supply limit or input/output test limits. In order to input the test data described 15 above, the user would select the power supply limits, and the Supply Menu Screen of Fig. 3E would appear. This menu was already described in detail above with regard to the DC test example and will not be described again.

20 Upon completing the Supply Menu Screen of Fig. 3E, the user again will be presented with the Data Entry Selection List. The user now selects the AC Test Limit Menu and the screen shown in Fig. 3I will appear. In order to supply the data for Fig. 3I, the user first 25 supplies an 8 character test name which will be used to identify the test being specified. The "DIAGNOSTIC #" field is pre-initialized to "01". The "DIAGNOSTIC #" will be used for failure correlation and the user can modify this number. The "POWER SUPPLY CASE #" field is 30 set to "1", indicating which of the configurations of the power supply screen is to be used for this test. The "CYCLE TIME" field is the cycle time for the test, and according to the above example 100ns would be placed therein. The "PIN TIMINGS" field contains pulse 35 information needed to perform the requisite AC test. Continuing with the AC test example, product read pin would have a  $T_{ON}$  of 0ns,  $T_{OFF}$  of 20ns and would be a

return to zero pulse ( $R_Z$ ). For illustrative purposes assume product read pin is R1. The write pin (assumed to be called W1) would be defined in an identical manner.

5 The "POWER/INPUT/OUTPUT PIN" field would then be filled in as follows: "PIN" : Vcc, "VALUE" : .0V, "PIN" : V<sub>BB</sub>, "VALUE" : -2V, "PIN" : V<sub>EE</sub>, "VALUE" : -5V. The "PATTERN GROUP" field would be set to "1 CYCLE/CELL" for the AC Test example. Other acceptable pattern group fields are  $N^2$ , 4 cycle/cell, etc, corresponding to well known test patterns. The "TOTAL PASSES" field would be set to 2. This field is used by the test system to determine the number of additional pass screens (to be described with regard to Fig. 3J). A 10 pass is defined as the number of operations to be performed during a test cycle. The pass number field is a digit identifying this operation cycle. The "CMODE" field describes whether the current addressing is to be in an incremental or decremental fashion. In 15 the present example, it would be incremental.

20

Continuing with the description of Fig. 3I, the "CADDRESS DIRECTION" field indicates the addressing scheme for processing through the array. In the above 25 AC Test Example it is rippling through the word address (ripword). The "HMODE" and "HADDRESS DIRECTION" have the same meaning as previously described only refer to  $N^2$  home array addresses. The " $N^2$  skip word" and " $N^2$  SKIP BIT" field are used if a reduced  $N^2$  or ping-pong 30 test is desired. If a reduced rather than a complete  $N^2$  is to be done, these fields will define the reduced addressing scheme by indicating the number of words or bits to be skipped when jumping through the array addresses.

The pulse section (lower third of Fig. 3I) identifies 35 which pins are to be pulsed during the pass. In the AC Test Example specified above, the first pass is a write cycle, so the write pin (W1) would be pulsed.

Finally, the function section at the bottom of Fig. 3I specifies the array operation to be performed. Since the AC Test Example is a single cycle per cell test, a single array operation is performed in the first pass.

5 Thus, for the AC example described above, "WX0" would be specified. The permissible functions are contained in Table 2. Thus, the user could enter multiple functions from Table 2 indicating distinct operations per cell for this pass through the array. Each of

10 these functions are well known in the testing art and will not be elaborated in detail.

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## TABLE 2

## AC PATTERN FUNCTIONS:

1)	READ UNIFORM ZERO:	RU0
2)	READ UNIFORM ONE:	RU1
5	3) READ CHECKERBOARD STARTING WITH ZERO:	RX0
	4) READ CHECKERBOARD STARTING WITH ONE:	RX1
	5) READ SINGLE BIT STARTING WITH ZERO:	RS0
	6) READ SINGLE BIT STARTING WITH ONE:	RS1
	7) READ DATA-IN BARS STARTING WITH ZERO:	RDO
10	8) READ DATA-IN BARS STARTING WITH ONE:	RD1
	9) READ COLBARS STARTING WITH ZERO:	RC0
	10) READ COLBARS STARTING WITH ONE:	RC1
	11) READ ZERO AT HOME ADDRESS:	RHO
	12) READ ZERO AT AWAY ADDRESSES:	RA0
15	13) READ ONE AT HOME ADDRESS:	RH1
	14) READ ONE AT AWAY ADDRESSES:	RA1
	15) WRITE UNIFORM ZERO:	WU0
	16) WRITE UNIFORM ONE:	WU1
	17) WRITE CHECKERBOARD STARTING WITH ZERO:	WX0
20	18) WRITE CHECKERBOARD STARTING WITH ONE:	WX1
	19) WRITE SINGLE BIT STARTING WITH ZERO:	WS0
	20) WRITE SINGLE BIT STARTING WITH ONE:	WS1
	21) WRITE DATA-IN BARS STARTING WITH ZERO:	WD0
	22) WRITE DATA-IN BARS STARTING WITH ONE:	WD1
25	23) WRITE COLBARS STARTING WITH ZERO:	WC0
	24) WRITE COLBARS STARTING WITH ONE:	WC1
	25) WRITE ZERO AT HOME ADDRESS:	WH0
	26) WRITE ZERO AT AWAY ADDRESSES:	WA0
	27) WRITE ONE AT HOME ADDRESS:	WH1
30	28) WRITE ONE AT AWAY ADDRESSES:	WA1

When the "FUNCTIONS" field of the AC Test Limit Screen of Fig. 3I have been filled in, the first pass of the checkerboard test has been completed. The data entry manager would automatically present an additional 5 pass screen (Fig. 3J). The total number of pass screens presented is a function of the "TOTAL PASS #" field of Fig. 3I. The fields in the additional pass screen of Fig. 3J have already been described in connection with AC Test Limit Screen of Fig. 3I and 10 will not be redescribed. The user would complete the additional pass screen of Fig. 3J for the "RX0" function. Upon completion, the Primary Option Menu of Fig. 3A will again appear. Since Options 1-4 have already 15 been completed, the user would select Option 5 to perform foreground processing. The Foreground Processing Screen of Fig. 3K would then appear. The Foreground Processing Screen of Fig. 3K directs the system to execute the auditor portion of the screen image manager and auditor program 26 and perform the data 20 integrity audits. These audits have been described previously and will not be redescribed here. Likewise, all of the fields in the Foreground Processing Screen of Fig. 3K have been described in connection with the AC Test Data Entry Screen of Fig. 3H and will not be 25 described again. Upon completion of foreground processing, the Primary Option Menu of Fig. 3A will again appear.

Following a successful on-line audit, Option 6 may be employed for background processing. Upon selection 30 of Option 6, the Background Option Menu of Fig. 3L will appear. The Background Processing Menu allows the user to direct the system to generate the universal language instruction sequence 16 of Fig. 1. The options fields merely require a yes/no response with the exception of 35 "TESTER". The generation of universal language source instruction sequence 16 will be described in detail below.

Universal Language Generator

Referring now to Fig. 5, the universal language generator will be described in detail. As shown in Fig. 5, universal language generator 14 comprises three 5 major modules; i.e., universal language generator controller 36, DC universal language generator 37, and AC universal language generator 38. Each major module will be described in more detail below.

The inputs to universal language generator 14 are 10 the data entry file 13 and the error message file 24 both of which have been described above with regard to interactive data entry.

Universal language generator controller 36 is the main routine controlling overall operation of universal 15 language generator 14. Controller 36 manages input/output data base operations, program entry/exit linkages, and system core allocations for internal processing by DC and AC language generators 37 and 38 respectively. Controller 36 also monitors (via return 20 codes) the success or failure of language generators 37 and 38. If encountering a failure it will select the appropriate message member from the partitioned error message file 24. The appropriate error message file member names along with a corresponding return code are 25 contained in an internal table in the controller. By matching the return codes from generators 37 and 38 with those of the table, the controller selects the corresponding error message member name. Controller 36 uses parameters triggered by the background processing 30 options (Fig. 3L) to determine which language generator to call.

Referring again to Fig. 5, the DC universal language generator 37 is a module which generates DC universal language statements. The organization and 35 internal components of DC universal language generator 37 are illustrated in Fig. 6.

Referring now to Fig. 6, the main routine in DC universal language generator 37 is the DC universal language generator controller 39. Controller 39 has the overall managing function for DC Product and DC Test Site universal language source generation. Controller 39 determines the major type of test requested (i.e., product or test site tests) from the DC array allocation screen of Fig. 3B. Based upon the type of test and the contents of data entry file 13, controller 39 determines which language source generator routines (41-49) to call and what order they are to be called in. Controller 39 also has responsibility for managing the entry/exit linkages among all the routines and monitoring, via return codes, the activities in each of the language source generators 41-49. Controller 39 also communicates appropriate errors and the generated universal language source statements to the main universal language generator controller 36.

Controller 39 first processes the supply menu of Fig. 3E and creates an internal power supply table which all generator routines 41-49 can access. The table is indexable by power supply case #. Each supply has 8 data fields associated with it. They are "ID", "VOLTAGE", "VALUE", "COMPLIANCE CURRENT", "MODE", "CLAMPING VOLTAGE", "SELECT INDICATOR" (Yes, No), and "ACTIVATE" (Yes, No). All of these fields except voltage value are directly discernible from the supply menu of Fig. 3E. "VALUE" is derived from the test limits data and will be described in that section. In addition, the "IO CLAMP" and "IO RANGE" will be saved in commonly accessible storage areas for insertion in the FRCPN statement when FRCPN generator 46 is called.

Controller 39 will then operate on the DC product test limits data of Fig. 3F or the DC test site limits data of Fig. 3G as stored in the data entry file 13, and create internal tables and commonly accessible storage areas which contain this information and can be

accessed by any of the universal language generator routines 41-49. The "TEST NAME", "DIAGNOSTIC #", MEASURED PIN", "HIGH AND LOW LIMITS" and "POWER SUPPLY CASE NUMBER" from either limits screen is saved in a common storage area. Controller 39 will construct an internal input/output state table and a write table array from the remaining screen information. The internal input/output state table will be organized with two entries per pin for all non power supply pins. The entries are "PIN NAME" and "VALUE". The pins which have power supply ID names will have their values compared against values already in the internal power supply table for the power supply case number requested. This will be done by matching the supply and if the values are different, the supply will have the new value inserted and the select set to yes. All supplies appearing in the screens regardless of value will have the activate indicator set.

The write table array will be built from the write information in the limits screen. There will be five entries per pin. The entries are "PIN NAME", "LEADING EDGE OF TRANSITION", "TRAILING EDGE OF TRANSITION", "DC/AC OR NONE", and "RETURN OR NON-RETURN TO ZERO". In addition a write flag will be set in an internal common area.

After the above described processing is completed, controller 39 calls INIT generator 48 to generate TSTID, COMMENT, and DMODE statements. Upon returning from INIT, controller 39 calls SELPS generator 41. This generator determines which if any SELPS statements need to be issued. Upon return from SELPS generator 41, ACTPS generator 42 is called. Following ACTPS, controller 39 calls FRCPN generator 46. Next controller 39 examines the write flag to determine if a write is required. If so it will call WRTPN generator 43. Next DELAY generator 45 will be called. Finally, controller 39 examines the pin to be measured. If it

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is a power supply, it will call MEAPS generator 44, otherwise it will call MEAPN generator 47.

Referring again to Fig. 6, the generator routines 41-49 will now be individually described. The DC universal language instruction set is described in Table 3. Table 3 includes a description of each DC universal language instruction, the purpose thereof, field definitions and a typical example. Each universal language instruction is referenced to the associated generator routine of Fig. 6. Immediately following Table 3, a detailed description of each universal language instruction and the source of the field data contained therein will be presented.

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TABLE 3  
DC UNIVERSAL LANGUAGE INSTRUCTION SET

GENERATOR ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
41	<u>SELPS</u> , P1, P2, P3, P4, P5 Purpose: Define a power supply	<p>P1 - power supply ID</p> <p>P2 - voltage and units</p> <p>P3 - compliance current and units</p> <p>P4 - mode of operation: i.e., standard/multiple/dual</p> <p>P5 - clamping voltage</p> <p>Example: SELPS V<sub>BB</sub> 0V 1A STANDARD 5V</p>
42	<u>ACTPS</u> , P1 Purpose: Activate a previously selected power supply	<p>P1 = power supply ID</p> <p>Example: ACTPS V<sub>BB</sub></p>

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**GENERATOR**

<b>ROUTINE</b>	<b>INSTRUCTION SYMBOL AND PURPOSE</b>	<b>FIELD DEFINITIONS AND EXAMPLE</b>
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<b>44</b>	<b><u>MEAPS</u>, P1, P2, P3, P4, P5, P6</b>	P1 - power supply ID P2 - mode of operation: i.e., standard/multiple/dual  P3 - flag:  Flag Value H - high limit only measurement Flag Value L - low limit only measurement Flag Value B - both high and low measurement P4 - high measurement value and units P5 - low measurement value and units P6 - diagnostic # used to assign error
-----------	---------------------------------------------	-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

Example:

MEAPS STANDARD B 500 $\mu$ A 180 $\mu$ A 20

<b>46</b>	<b><u>FRCPN</u>, P1, P2, P3, P4</b>	P1 - value and units P2 - range and units P3 - clamping condition and units P4 - pin or pins to be forced
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Example:

FRCPN 700mV 10mA 2.5V A02

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ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
47	<u>MEAPN</u> , P1, P2, P3, P4, P5 Purpose: Measure an I/O pin	P1 - Flag: Flag Value H - High limit only measurement Flag Value L - low limit only measurement Flag Value B - both high and low measurement P2 - high measurement value and pin P3 - low measurement value and pin P4 - diagnostic # used to assign error conditions P5 - pin or pins to be measured

## GENERATOR

ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
4.3	WRTPN, P1, P2, P3, P4  Purpose: Cause write clock pin to apply a transition	P1 - write clock pin  Flag Value 1 - DC, return to zero, negative polarity  Flag Value 2 - DC, return to zero, positive polarity  Flag Value 3 - DC, non-return to zero, negative polarity  Flag Value 4 - DC, non-return to zero, positive polarity  Flag Value 5 - AC, return to zero, negative polarity  Flag Value 6 - AC, return to zero, positive polarity  Flag Value 7 - AC, non-return to zero, negative polarity  Flag Value 8 - AC, non-return to zero, positive polarity  P3 - leading edge value and units P4 - trailing edge value and units

Example:

WRTPN A01 7 -600mV -1200mV

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GENERATOR ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
45	<u>DELAY</u> , P1 Purpose: Delay between test instruction execution	P1 - amount of delay and units Example: DELAY 8mS
48	<u>TSTID</u> , P1 Purpose: Identify type of test statements	P1 - AC/DC Example: TSTID DC
49	<u>COMMENT</u> , P1 Purpose: Informational command	P1 - comment Example: COMMENT TEST ABC
48	<u>DMODE</u> , P1 Purpose: Identify diagnostic mode	P1 - on/off Example: DMODE OFF

Referring now to Fig. 6 and Table 3, SELPS generator routine 41 builds all SELPS universal language statements. This statement defines a power supply. The routine accesses the power supply case number and 5 uses it to index into the previously described internal power supply table. The select indicator for all supplies in this case will be examined to determine if a supply needs to be selected. If selection is needed, the routine uses information previously saved in the 10 internal power supply table to construct a SELPS statement.

ACTPS generator routine 42 builds the ACTPS universal language statement. This statement is used to activate a previously selected power supply. The 15 power supply ID field is derived from the internal supply table and the entries of the table with activate=yes have an ACTPS generated from them.

WRTPN generator 43 builds the WRTPN universal language statement. This statement causes a write 20 clock pin to apply a transition. Generator 43 processes the write information which originated in the write section of the DC test limit records (Fig. 3F) and is saved in the internal write table. The specified 25 information includes the write clock pin, the leading and trailing transition edges, and whether it is a transitory pulse. The routine will determine the polarity (negative or positive) of the transition or pulse by comparing the edges. It processes through the internal write table entries previously described and 30 based on the combination of information in these entries sets a flag in the WRTPN statement. The various combinations are described in Table 3 under the WRTPN statement.

MEAPS generator routine 44 builds the MEAPS 35 universal language statement. This statement measures a power supply. The routine obtains the power supply to be measured, the high and low values and the

diagnostic number from data originating in the test limits records of Fig. 3For 3G. The mode is derived from an internal supply table. For the power supply case being used, the power supply being measured is 5 matched against the supplies in the table and the appropriate mode selected. Values are determined based on whether both high and low limits is specified in the test limits screen or only one or the other.

10 DELAY generator routine 45 builds a DELAY universal language statement. This statement is used to identify the delay between execution of test instructions. Routine 45 calculates the required delay based on the types of instructions to be used and the number of instructions. Each type of instruction contributes 15 a specific amount of delay. The DC universal language generator controller 39 will indicate by means of a parameter whether an override delay is to be used instead of the calculated delay. The amount of override delay originates from the test limit record of 20 Fig. 3F.

25 FRCPN generator routine 46 builds the FRCPN universal language statement. This statement is used to apply forcing conditions to input/output pins. The routine constructs and maintains an internal history state table containing the input/output pins and the values to be applied. Routine 46 analyzes the I/O state table constructed by controller 39 and compares the value of each pin in the I/O state table against its corresponding entry in the internal history state 30 array table. Pins with the same values are removed from the I/O state table. Non matching new pins are added to the history table. After completing a pass through the I/O state table the pins that remain are grouped according to common value to be forced. All 35 unique values will have a FRCPN statement issued. The range and clamping conditions are derived from data originating in the supply record of Fig. 3E.

MEAPN generator routine 47 builds the MEAPN universal language statement. This statement is used to measure an output pin. The routine processes the measurement information which originated in the limits 5 records of Figs. 3F and 3G. The specified information includes the measured pin, the high and low limits, and the diagnostic number.

The INIT generator routine 48 builds the TSTID and DMODE universal language statements. Between construction 10 of these statements "COMMENT" is called and the test name address passed to it. The TSTID instruction identifies the type of tests being done and the DMODE instruction identifies whether diagnostic mode stop on first fail is requested or whether the tester is to 15 continue even if a failure occurs. The routine saves the DC identifier in the TSTID statement. The diagnostic number saved in a common area by controller 39 is used to determine the diagnostic mode and either an on or off condition will be saved. If the diagnostic 20 number is 0, then "OFF" will be set; otherwise, it will be "ON".

The COMMENT generator routine 49 builds the COMMENT universal language statement. This statement is used to communicate a comment. The routine uses an 25 address parameter passed to it pointing to the comment to be used. COMMENT routine can be called by any other routine. For example, it may be called by INIT routine 48 to generate a test name comment statement.

Referring again to Fig. 5, the AC universal 30 language generator 38 is a module which generates AC universal language statements. The organization and internal components of AC universal language generator 38 is illustrated in Fig. 7. Referring now to Fig. 7, the main routine in AC universal language generator 38 35 is the AC universal language generator controller 50. Controller 50 has the overall managing function for AC product universal language source generation. Based

upon the type of test and the contents of data entry file 13, controller 50 determines which language source generator source routines (51-66) to call and in what order they are to be called. Controller 50 also has 5 responsibility for managing the entry/exit linkages among all the routines and monitoring, via return codes, the activities in each of the language source generators 51-66. This monitoring process includes communicating both appropriate errors as well as any 10 universal language source statement built by a source language generator 51-66 to the universal language generator controller 36.

Controller 50 first constructs an internal power supply table from the supply menu of Fig. 3E. This 15 table is accessible by any of generator routines 51-66 and is indexable by power supply case number. Each supply has seven data fields associated with it. They are "ID", "VOLTAGE VALUE", "COMPLIANCE CURRENT", "MODE", "CLAMPING VOLTAGE", "SELECT INDICATOR" 20 (Yes/No), and "ACTIVATE" (Yes/No). All of these fields except "VOLTAGE VALUE" are derived from the test limits data and will be described in that section. Controller 50 then processes the AC limits screen of Fig. 3I. The "TESTNAME", "DIAGNOSTIC #", "POWER SUPPLY CASE #", and 25 "CYCLE TIME" will be saved in commonly accessible storage areas to be used by any of generator routines 51-66. An internal pin timing table is constructed from the timing information specified in the test menu. There are five table elements per pin. They are "PIN 30 NAME", "TURN-ON TIME", "TURN-OFF TIME", "RETURN OR NON-RETURN TO ZERO" and "SELECT" (Yes/No). All pins in the menu will be matched against the pins and values already in the pin timing table. Pins which match and whose values are the same will have "SELECT" set to 35 "NO" and will not be respecified by PGTIM Generator 56. The dissimilar values will be inserted into the table and "SELECT" set to "YES". Non-matching pins will be

added to the internal pin timing table as new and have "SELECT" set to "YES".

5 The "PIN/VALUE" section of the test menu will then be processed. Controller 50 will construct an internal INPUT/OUTPUT state table array with two entries per pin for all non power supply pins. The entries are "PIN NAME" and "VALUE". Pins which have power supply ID names will have their values compared against values already in the internal power supply table for the 10 power supply case number indicated in the commonly accessible storage area. This is done by matching the supply ID pin names. If the values are different the supply will have the new value inserted and the select set to yes. All supplies appearing will have the 15 activate indicator set.

20 The pattern section is processed next by controller 50. The "PATTERN GROUP", "TOTAL PASSES", "PASS #", "CMODE", "CADDRESS DIRECTION", "HMODE", "HADDRESS DIRECTION", "N<sup>2</sup> SKIP WORD", and "N<sup>2</sup> SKIP BIT" fields are all saved in commonly accessible internal storage areas. An internal pulse table is constructed from the pulse section of the menu. This table has one element per pin, i.e., the pin name.

25 The function section is processed next. The three character function operations illustrated in Table 2 are saved in a function table with each function being an element. Also a count of the number of functions is kept and saved in a commonly accessible storage area to be used by the PASDEL routine 59. TSTID routine 66 is 30 then called and after its completion controller 50 will call the COMMENT routine 61 passing to it the address of the commonly accessible storage area containing the test name. Next DIMEN generator 51 followed by SELPS generator 54 will be called. SELPS generator 54 35 determines which if any SELPS statements need be issued. ACTPS routine 53 will be called next followed by PGTIM routine 56. These routines will determine

which if any ACTPS and PGTIM statements need be issued. CYCTM routine 55 will be called next. Following CYCTM, controller 50 will call TEXEC and DELAY generators 64 and 57, respectively. It will then call COMMENT generator 61 passing it the address of the commonly accessible storage area containing the pattern group. 5 PATDEL routine 58 followed by PASDEL routine 59 will be called next.

Controller 50 will then analyze the function table 10 elements one at a time. It will key off the first character to determine whether to call READ or WRITE routines 63 or 65, respectively. "W" indicates write and "R" indicates read. The correct routine will be passed the address of the function table element. 15 After finishing processing through the function table the PLSPN routine 62 will be called. This completes the processing for the menu of Fig. 3I.

Controller 50 then examines the total passes field 20 specified to see if any Fig. 3J menus are required. The controller will process Fig. 3J menus until the total pass field is satisfied. This processing consists of saving the "PASS #", "CMODE", "CADDRESS 25 DIRECTION", "HMODE", "HADDRESS DIRECTION", "N<sup>2</sup> SKIP WORD" and "N<sup>2</sup> SKIP BIT" fields in commonly accessible internal storage areas. Internal pulse table and 30 function tables are constructed as previously described. Starting with a call to PASDEL generator 58, the remaining controller processing is the same as previously described for the menu of Fig. 3I. This is the same for all Fig. 3J menus.

Referring again to Fig. 7, generator routines 35 51-66 will now be individually described. Each generator routine generates a single universal language statement type. The AC universal language statement types are described in Table 4. Table 4 includes a description of each AC universal language statement, the purpose thereof, field definitions and a typical

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example. Each universal language statement is referenced to the associated generator routine of Fig. 7. Immediately following Table 4, a detailed description of each universal language instruction and the source of the field data contained therein will be presented.

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TABLE 4  
AC UNIVERSAL LANGUAGE STATEMENTS

GENERATOR	ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
5	<u>TSTID, P1</u>	P1 - AC/DC	
	Purpose: Identify type of test statements	Example: TSTID, AC	
10	<u>DIMEN, P1, P2, P3, P4, P5, P6</u>	P1 - # of word address lines P2 - # of bit address lines P3 - # of control lines P4 - # of data in lines P5 - # of data out lines P6 - Eflag	
	Purpose: Communicate array dimension and related information	Flag 1 - interwoven Flag 2 - non interwoven	
15		Example: DIMEN 7 4 6 10 10 2	

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ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
54	<u>SELPS</u> , P1, P2, P3, P4, P5	See Table 3, Generator Routine 41
53	<u>ACTPS</u> , P1	See Table 3, Generator Routine 42
55	<u>CYCTM</u> , P1	P1 - value and units
	Purpose: Specify cycle time for the test being applied	Example: CYCTM 10NS
57	<u>DELAY</u> , P1	See Table 3, Generator Routine 45

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ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
56	<u>PGTIM</u> , P1, P2, P3, P4 Purpose: Establish timing conditions	<p>P1 - pin name P2 - Flag</p> <p>Flag Value 1 - negative pulse, return to zero</p> <p>Flag Value 2 - negative pulse, non- return to zero</p> <p>Flag Value 3 - positive pulse, return to zero</p> <p>Flag Value 4 - positive pulse, non- return to zero</p> <p>P3 - pulse width and units P4 - start time and units</p>

Example:

PGTIM A03 3 10NS 0NS

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GENERATOR ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
58	<u>PATDEL, P1</u> Purpose: Identify start of specific patterns for a unique AC test	P1 - numeric which identifies the group of patterns in this test 1 - 1 cycle/cell 2 - 4 cycle/cell 3 - $N^2$ 4 - reduced $N^2$

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GENERATOR ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
59	<u>PASDEL</u> , P1, P2 Purpose: Delineate a unique set of array operations within a group of array patterns	P1 - numeric pass # (starts at 1 for each unique group of patterns) P2 - # of read/write operations/cell
	Example: PASDEL 1 4	
62	<u>PLSPN</u> , P1 Purpose: Apply a pulse to a control line during a group of patterns	P1 - control pin or pins Example: PLSPN A05
60	<u>LOGST</u> , P1, P2 Purpose: Apply a value to a control line or lines during a group of AC test patterns	P1 - value, units P2 - control pin or pins Example: LOGST 2V A05

## GENERATOR

ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
63	<u>READ</u> , P1, P2, P3, P4, P5, P6, P7	P1 - current array address flag and away address flag for N <sup>2</sup> patterns

Purpose: Read a value from an array

Flag Value 1 - ripple word address direction

Flag Value 2 - ripple bit address direction

Flag Value 3 - word direction only

Flag Value 4 - bit direction only

Flag Value 5 - grey code word direction

Flag Value 6 - complemented grey code word direction

Flag Value 7 - N<sup>2</sup> skip

P2 - current address sequence flag

Flag Value 1 - increment

Flag Value 2 - decrement

P3 - home address flag for N<sup>2</sup> patterns

Flag Value 0 - no action

Remaining breakdown is the same as for P1

P4 - home address sequence flag

Flag Value 0 - no action

Flag Value 1 - increment

Flag Value 2 - decrement

P5 - data type and start value flag

Flag Value 1 - uniform 0

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ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
63 Con't.		

Flag Value 2 - uniform 1  
Flag Value 3 - checkerboard 0  
Flag Value 4 - checkerboard 1  
Flag Value 5 - Onebit 0  
Flag Value 6 - Onebit 1  
Flag Value 7 - data-in bars 0  
Flag Value 8 - data-in bars 1  
Flag Value 9 - colbars 0  
Flag Value 10- colbars 1  
P6 - word address amount to be skipped  
for N<sup>2</sup> skip  
P7 - bit address amounts to be skipped  
for N<sup>2</sup> skip

Example:

READ 1 1 0 0 1 0 0

## GENERATOR

ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
65	<u>WRITE</u> , P1, P2, P3, P4, P5, P6, P7	P1 - current array address flag and away address flag for $N^2$ patterns  Purpose: Write a value into an array  Flag Value 1 - ripple word address direction Flag Value 2 - ripple bit address direction  Flag Value 3 - word direction only Flag Value 4 - bit direction only Flag Value 5 - grey code word direction Flag Value 6 - complement grey code word direction  Flag Value 7 - $N^2$ skip P2 - current address sequence flag Flag Value 1 - increment Flag Value 2 - decrement P3 - home address flag for $N^2$ patterns Flag Value 0 - no action Remaining breakdown is the same as P1 P4 - home address sequence flag Flag Value 0 - no action Flag Value 1 - increment Flag Value 2 - decrement P5 - data type and start value flag Flag Value 1 - uniform 0 Flag Value 2 - uniform 1

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GENERATOR ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
65 Con't.		<p>Flag Value 3 - checkerboard 0 Flag Value 4 - checkerboard 1 Flag Value 5 - onebit 0 Flag Value 6 - onebit 1 Flag Value 7 - data-in bars 0 Flag Value 8 - data-in bars 1 Flag Value 9 - colbars 0 Flag Value 10- colbars 1</p> <p>P6 - word address amount to be skipped for N<sup>2</sup> skip</p> <p>P7 - bit address amount to be skipped for N<sup>2</sup> skip</p>

Example:

WRITE 1 1 0 0 1 0 0

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GENERATOR	ROUTINE	INSTRUCTION SYMBOL AND PURPOSE	FIELD DEFINITIONS AND EXAMPLE
	<u>64</u>	<u>TEXEC, P1, P2</u>	P1 - execution flag Flag Value 1 - execute until 1st fail is reached Flag Value 2 - execute regardless of number fails P2 - diagnostic fail #
		Example: TEXEC 1 0 25	Example: COMMENT TEST ABC

Referring now to Fig. 7 and Table 4, DIMEN Generator Routine 51 builds the DIMEN universal language statement. This statement communicates the array size and related general information. Routine 51 reads the 5 AC array allocation menu of Fig. 3C and saves the number of word, bit, data, and control lines in the DIMEN statement. In addition the type of design (interwoven or noninterwoven) is translated into a flag field in the DIMEN statement.

10 ACTPS Generator Routine 53 builds the ACTPS universal language statement. This routine has been previously described with regard to Routine 42 of Fig. 6. The same routine is used here.

15 SELPS Generator Routine 54 builds the SELPS universal language statement. This routine has been previously described with regard to Routine 41 of Fig. 6. The same routine is used here.

20 CYCTM Generator Routine 55 builds the CYCTM universal language statement. This statement specifies the cycle time for the test being applied. Routine 55 uses the cycle time saved by controller 50 in the commonly accessible storage area.

25 PGTIM Generator Routine 56 builds the PGTIM universal language statement. This statement specifies the timing conditions to be used for the test. Routine 56 uses internal timing history tables, built by controller 50, derived from the AC Test Limits Record of Fig. 3I. The routine will analyze the select field for each pin in the pin timing table and construct a 30 PGTIM statement for each one which is yes. The pin name and start time come directly from table fields. The pulse width is the absolute difference between the start and stop time fields in the timing table array. The flag is set based on the combination of return or 35 non-return to zero and plus or minus polarity. A positive polarity will have a stop time greater than start time and a negative will be the opposite. The

return or non-return to zero is indicated in the timing table.

5       DELAY Generator Routine 57 builds the DELAY universal language statement. This routine has previously been described with regard to Routine 45 of Fig. 6. The same routine is used here.

10      PATDEL Generator Routine 58 builds the PATDEL universal language statement. This statement identifies the start of an array test pattern set. Routine 15 contains an internal table which contains a pattern group name and a pre-assigned numeric integer. Matching is performed between the pattern group name saved by the controller from the AC test limit record of Fig. 3I and the names in the internal table array. The corresponding integer is selected.

20      PASDEL Generator Routine 59 builds the PASDEL universal language statement. This statement delineates a unique set of array operations within a group of array patterns. Routine 59 uses a counter which is initialized to 1 at the start of each new pattern group. The counter is updated for each new pass within a pattern group as directed by the AC test limit records of Figs. 3I and 3J. Routine 59 also examines the counter built by controller 50 indicating the 25 number of read/write array operations to be performed for this pass. These above two counters are then saved in the PASDEL statement.

30      LOGST Generator Routine 60 builds the LOGST universal language statement. This statement indicates that a logic pre-conditioning value to a control line or lines during a pass of an AC array test has been requested. The routine uses an I/O state table built by controller 50. It analyzes the table and groups the pins with a common value together. All unique values 35 will have a LOGST issued.

COMMENT Generator Routine 61 builds the COMMENT universal language statement. This routine has been

previously described in connection with Routine 49 of Fig. 6. The same routine is also used here.

PLSPN Generator Routine 62 builds the PLSPN universal language statement. This statement applies a 5 pulse to a control line during an array test pass. Routine 62 derives the control lines to be pulsed from the internal pulse table built by controller 50.

READ Generator Routine 63 builds the READ universal language statement. This statement reads a value 10 from an array. Routine 63 first constructs a current array address or away N<sup>2</sup> address flag. This is done by matching the caddress direction saved in a commonly accessible storage area by controller 50 against an internal table containing supported directions and 15 corresponding flag values. Table 4 indicates the supported caddress directions and the corresponding flag values. The current address sequence flag value is derived from the cmode field saved in a common storage area by controller 50. Increment has a value 20 of 1 and decrement a value of 2. The home address flag specifies the home addressing direction for N<sup>2</sup> type tests only. The flag is constructed using the same matching technique and address table previously discussed above. A field value of 0 is set if this is not 25 specified in the menu. The home address sequence flag is defined only for N<sup>2</sup> processing and is derived from the hmode field saved by controller 50. The processing is similar to cmode only; a value of 0 is used if this field is not in the menu. The data type and start 30 value flag is built by first selecting the read operation from the function table built by controller 50. The address of this function table element is passed from controller 50. A matching is performed comparing this operation against a table containing supported 35 read operations and corresponding flag value. Table 2 shows the supported read operations. The corresponding flags are shown in Table 4. The N<sup>2</sup> skip values for the

word and or bit address directions derived from the AC test limits screens (Figs. 3I, 3J) were saved by controller 50. These skip values are used when performing reduced  $N^2$  tests to allow selected away address processing. The above described flags and skip values are saved in the READ statement.

The TEXEC Generator Routine 64 builds the TEXEC universal language statement. This statement contains the test execution diagnostic information. Routine 64 sets a flag to indicate if the test is to stop when the first error is found or continue. If the diagnostic number, saved in a common area by the controller 50 is not 0, then the flag will indicate stop on first error. The diagnostic number will also be inserted in the TEXEC statement. The diagnostic fail number is derived from the AC test limits screen (Fig. 3I).

WRITE Generator Routine 65 builds the WRITE universal language statement. This statement writes a value into an array. Routine 65 first constructs a current array address or away  $N^2$  address flag. This is done by matching the caddress direction saved in a commonly accessible storage area by controller 50 against an internal table containing supported address directions and corresponding flag values. Table 4 indicates the supported caddress directions and the corresponding flag values contained in the internal table. The current address sequence flag value is derived from the cmode field saved in a commonly accessible storage area by controller 50. Increment has a value of 1 and decrement a value of 2. The home address flag is used to specify the home address direction for  $N^2$  tests. The flag is only used for  $N^2$  type tests. The flag is constructed using the same matching technique and address table discussed above. A flag field of 0 is set if this field is not specified in the menu. The home address sequence flag is defined only for  $N^2$  tests and is derived from the hmode field

5 saved by controller 50. The processing is similar to cmode; only a 0 flag value is saved if the data is not in the menu. The data type and start value flag is built by first selecting the write operation from the  
10 function table array. The address of this function table array element is passed from controller 50. A matching is performed comparing the operation against a table supported write operations and corresponding flag values. Table 2 shows the supported WRITE operations  
15 and the corresponding flags are shown in Table 4. The  $N^2$  skip values for the word and/or bit address directions derived from the AC test limit records of the data entry file (Figs. 3I, 3J) are also saved. These skip values are used when performing reduced  $N^2$  tests  
15 to allow selected away address processing.

TSTID Generator Routine 66 builds the TSTID universal language statement. This statement identifies the type of test being done. The routine saves the AC identifier in the TSTID statement.

20 Referring again to Fig. 5, universal language instruction sequence 16 is comprised of a combination of the DC and AC universal language statements described above in connection with Tables 3 and 4, respectively. The statements are sequenced to perform  
25 a specified DC or AC test, and sequences of statements are repeated a sufficient number of times to perform all of the DC and AC tests specified by the user. Tables 5, 6, and 7 provide examples of the universal language instruction sequences used to perform the DC  
30 Product Test, DC Test Site Test and AC Test which were illustrated as examples in the "Interactive Data Entry" section above.

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TABLE 5  
DC PRODUCT TEST EXAMPLE  
UNIVERSAL LANGUAGE INSTRUCTION SEQUENCE

	TSTID	DC				
5	COMMENT	TEST 1				
	DMODE	ON				
	SELPS	VCC	2V	1A	STANDARD	2V
	SELPS	VBB	0V	1A	STANDARD	2V
	ACTPS	VCC				
10	ACTPS	VBB				
	FRCPN	800mV	10MA		2.0V	P2, P3
	FRCPN	200mV	10MA		2.0V	P1
	DELAY	8mS				
	MEAPN	B	500 $\mu$ A	100 $\mu$ A	1	P1

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TABLE 6  
DC TEST SITE EXAMPLE  
UNIVERSAL LANGUAGE INSTRUCTION SEQUENCE

	TSTID	DC					
5	COMMENT	TEST 2					
	DMODE	ON					
	FRCPN	-10 $\mu$ A	100 $\mu$ A	10V	P1		
	FRCPN	GND	100 $\mu$ A	10V	P2, P3		
	DELAY	80mS					
10	MEAPN	B	-500mV	-700mV	1	P1	

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TABLE 7  
AC TEST EXAMPLE  
UNIVERSAL LANGUAGE INSTRUCTION SEQUENCE

TSTID	AC
5	COMMENT TEST 3
	DIMEN 7 4 6 10 10 2
	SELPS VCC 0V 1A STANDARD 2V
	SELPS VBB -2V 1A STANDARD 2V
	SELPS VEE -5V 1A STANDARD 2V
10	ACTPS VCC
	ACTPS VBB
	ACTPS VEE
	PGTIM R1 3 20ns 0ns
	PGTIM W1 3 20ns 0ns
15	CYCTM 100ns
	TEXEC 1 1
	DELAY 8ms
	COMMENT 1 CPC
	PATDEL 1
20	PASDEL 1 1
	WRITE 1 1 0 0 3 0 0
	PLSPN W1
	PASDEL 2 1
	READ 1 1 0 0 3 0 0
25	PLSPN R1

Universal to Tester Translator Selector

Referring again to Fig. 1, the details of universal to tester translator selector 18 will now be described. Translator selector 18 selects the proper 5 universal to tester translator 19 for translation of the universal language instruction sequence 16. The translator selector 18 is activated by appropriately selecting the DC or AC Test Instruction Set option on the Background Processing Screen (Fig. 3L).

10 The translator selector 18 operates upon universal language source file 16, parameter file 15 and tester footprint file 17. Parameter file 15 includes data which may be obtained during interactive data entry relating to product type, part number identification, 15 technology identification and the name of the tester to be employed. Tester footprint file 17 contains the correspondence between a particular tester's channels and the physical input/output/power supply pins on the product. There is one footprint file for each product 20 for each tester on which the product will be tested. The footprint is created once per product and then saved.

Translator selector 18 ensures that it can link to the particular translator 19 being called out in 25 parameter file 15 and ensures that there is a footprint for the tester and for the product from the footprint file 17. Once these checks are complete, the translator selector 18 will link to the proper translator 19.

It will be recognized by those having skill in the 30 art that the data for parameter file 15 and tester footprint file 17 may be entered during the interactive data entry phase (described above) or may be entered prior to or after the interactive data entry phase. Moreover, it will also be realized by those having 35 skill in the art that the universal to tester translator selector 18 need not be a computer program per se. Specifically, selection of the appropriate translator

19A...19X may be performed by the operator who physically links the appropriate translator to the universal language source file 16. In that case, the operator would have to provide an appropriate tester footprint file to the selected translator.

Whether done manually by the operator or automatically by translator selector 18, the universal language instruction sequence 16, appropriate parameters from parameter file 15, and an appropriate tester footprint file 17 are made available to the selected translator 19A...19X.

#### Universal to Tester Translator

Referring now to Fig. 8, the details of a typical universal to tester translator 19 is described. Fig. 8 illustrates a typical translator 19. However, it will be realized by those having skill in the art that for other testers, the configuration of translator 19 may vary.

Referring again to Fig. 8, translator 19 includes an input manager 67 which serially reads universal language instructions from universal language instruction sequence 16 and appropriately links to DC setup generator 77, AC setup generator 74 or otherwise processes the universal language source statement. Input manager 67 also performs the initial processing of the footprint and parameter file (17 and 15, respectively) and creates a small readily usable file 73 of parameter and footprint data. It also adds selected universal language statement data to file 73, e.g., the data found in the DIMEN source statement (Table 4). This data is common to both DC and AC setup processors. Therefore, it is most expedient to have input manager 67 decompose this statement and make the data easily accessible by either processor. Input manager 67 also tracks where control is currently being retained so that when a universal language source statement

common to both AC and DC tests is encountered (e.g., the SELPS instruction), the proper processing and linkage thereof occurs.

DC setup generator 77 will be invoked whenever  
5 input manager 67 encounters a TSTID statement with its field specifying DC testing. DC setup generator 77 generates the necessary tester instructions for performing the DC tests specified in universal source file 16. The generated DC tester instructions are stored in  
10 DC setup file 78.

AC setup generator 74 is invoked when input manager 67 encounters a TSTID statement with its field specifying AC testing. AC setup generator 74 generates the necessary tester instructions for performing AC  
15 testing on the product. The appropriate AC tester instructions are stored in AC setup file 79. AC setup generator 74 also coordinates the invocation of bit pattern generator program 76 and monitors the patterns that have been created for timing and voltage test  
20 cases requested by the system user.

Notes file 75 is a communication vehicle between AC setup and bit pattern generators 74 and 76, respectively. Notes file 75 records each type of bit pattern test generated (checkerboard, 4 cycle/cell, ... etc.) and the kind of addressing specified for that test (increment/decrement, word major/bit major). Notes file 75 retains a copy of the relevant portions of the tester memory for each of these combinations and a directory so that any combination may be retrieved.  
25  
30 The appropriate data is retrieved from the Notes file 75 and written to the AC setup file 79 whenever a test is called for which bit patterns have already been generated. In this way common sets of patterns do not need to be continuously regenerated. The need for pattern re-use is common, for example, when the same  
35 pattern sequence is required for several voltage or timing cases.

Bit pattern generator 76 generates the particular bit patterns which cause the tester to systematically exercise the array memory cells. The dimension data stored in file 73 is employed by bit pattern generator 5 76 in order to generate bit patterns. Examples of such dimension data is the number of word address lines, the number of bit address lines, the number of control lines for the memory, etc. From this data and known characteristics of the tester, bit pattern generator 76 10 is able to generate many different bit patterns. Common bit pattern test data will be repeated on the bit pattern file each time a new AC setup is required. For example, the same 4-cycle per cell bit pattern test 15 may be required for each of four different voltage setups. In this case, the 4-cycle per cell bit patterns are repeated three times.

Output manager 82 generates the complete tester instruction set 30, by combining both AC setup 79 and DC setup 78 files.

20 In order to more particularly describe the detailed processing that occurs within translator 19 a hypothetical tester will now be described. Then, the manner in which translator 19 translates the universal language instruction sequence 16 into the hypothetical 25 tester instruction sequence will be described. It will be understood by those having skill in the art that every tester accepts a unique tester instruction set so that the design of a translator will be unique for every tester. It will also be realized by those having 30 skill in the art that different testers may accept a higher or lower level of instructions so that the translator design may be more simple or more complicated from that described here.

35 Referring now to Fig. 9, the hardware architecture of a typical general purpose memory tester is illustrated. Tester 21X is driven by an instruction sequence that controls both the operating system of the

tester and all the tests to be performed on array 25X. These instructions are stored in tester memory 84 via high speed buss 83. The tester is controlled by a microprocessor or other controller 86 and includes a 5 timing generator 87, data generator 88 and address generator 89. The appropriate tester instructions in tester memory 84 are transmitted to generators 87, 88 and 89 by controller 86 to thereby form sequences of binary voltage levels which are output to the array 10 under test 25X via drivers/receivers 91. The architecture of a typical tester 21 does not form a part of the present invention and will not be described in further detail.

15 In order to illustrate the translation of universal language instruction sequences into a tester instruction sequence 30, the translation of the universal language instruction sequences for the DC Product, DC Test Site and AC Test Examples of Tables 5-7, will now be described. Table 8 illustrates the DC Product 20 Test Example universal language instruction sequence (identical to Table 5) and the corresponding DC Product Test Example tester instruction sequence.

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Table 8

<u>DC PRODUCT TEST EXAMPLE</u>		<u>DC PRODUCT TEST EXAMPLE</u>
<u>UNIVERSAL LANGUAGE</u>		<u>TESTER INSTRUCTION SEQUENCE</u>
<u>INSTRUCTION SEQUENCE</u>		
5	TSTID DC	<div style="border-left: 1px solid black; padding-left: 10px; margin-left: 20px;">FF00 0701 XXXX 0702 XXXX ⋮ 0709 XXXX</div>
	COMMENT TEST 1	
10	DMODE ON	9201
	SELPS VCC 2V 1A STANDARD 2V	<div style="border-left: 1px solid black; padding-left: 10px; margin-left: 20px;">0204 0330 0844 0404 0330</div>
15	SELPS VBB 0V 1A STANDARD 2V	<div style="border-left: 1px solid black; padding-left: 10px; margin-left: 20px;">0202 0330 0842 0402 0000</div>
	ACTPS VCC	0641
	ACTPS VBB	0621
20	FRCPN 800MV 10MA 2.0V P2, P3	<div style="border-left: 1px solid black; padding-left: 10px; margin-left: 20px;">0AC2 0200 0BC2 0020 0DC2 3204 0AC3 0200 0BC3 0020 0DC3 3204</div>
25	FRCPN 200MV 10MA 2.0V P1	<div style="border-left: 1px solid black; padding-left: 10px; margin-left: 20px;">0AC1 0200 0BC1 0020 0DC1 0C84</div>

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DC PRODUCT TEST EXAMPLE  
UNIVERSAL LANGUAGE  
INSTRUCTION SEQUENCE

DC PRODUCT TEST EXAMPLE  
TESTER INSTRUCTION SEQUENCE

DELAY 8mS

9105 0008

5

MEAPN B 500 $\mu$ a 100 $\mu$ a 1 P1

{ 9301  
0C011F43  
0C020643  
17C1

The manner in which the DC Product Test Example universal language instruction sequence is processed by translator 19 to generate the DC Product Test Example tester instruction sequence (Table 8) will now be 5 described. Referring again to Fig. 1, universal to tester translator selector 18 determines the tester to be used and the product identification from parameter file 15 and accesses the corresponding tester footprint from tester footprint file 17. The appropriate translator 10 19 is selected and control is passed to input manager 67 (Fig. 8).

Referring again to Fig. 8, input manager 67 begins sequencing through the universal source statements in the left hand column of Table 9. The first statement 15 encountered is TSTID DC. Input manager 67 retains this entire statement until the next TSTID statement is encountered. With each subsequent read of a universal language source file statement, input manager 67 checks the statement symbol. If it is TSTID, input manager 67 20 replaces the old TSTID statement with the new TSTID. Control is linked to DC setup generator 77 or AC setup generator 74, and a tester setup instruction FF00 is issued. DC setup generator will do some preliminary 25 register setting (0701 XXXX, etc.), to anticipate DC testing environment. AC setup generator 74 will do the same, anticipating AC testing environment (0701 YYYY). The tester op codes are all represented in hexadecimal 30 on the right hand column of Table 8. If the statement symbol is not TSTID, the input manager links to either the AC setup or DC setup generator, depending upon the most recent TSTID value stored by input manager 67.

The next universal language source statement 35 encountered is the COMMENT statement. This is an optional informational aid only. The COMMENT data is printed to a system listing but is not further processed.

The next statement presented to DC setup generator 77 is the DMODE statement. This statement causes DC setup generator 77 to generate the op codes necessary to cause the tester to abort the DC test if a fail 5 occurs on any digital voltmeter compare. The next statement is a SELPS statement which defines a power supply. This statement causes the DC setup generator to load current compliance, current range and supply digital to analog converters for the appropriate power 10 supply. Table 8 shows the tester op code expansion done by DC setup generator 77 for both SELPS  $V_{CC}$  and SELPS  $V_{BB}$ . Each SELPS statement expands to 3 tester instructions. They are:

'02' load current compliance digital to analog  
15 converter  
'08' load power supply current range  
'04' load power supply digital to analog converter  
The tester power supply to be used is defined in  
the low-order 4 bits of tester instruction byte 2.  
20 Through the use of the footprint file 73, DC Setup  
Generator 77 is able to convert  $V_{CC}$  to power supply 4  
and  $V_{BB}$  to power supply 2. The high-order bit setting  
of byte-2 of tester instruction '08' indicates that the  
1 amp current range will be used. The value portions  
25 of tester instructions '02' and '04' (bytes 3 and 4)  
are generated based upon a 12-bit digital to analog  
converter power supply table:

Bit 15: + 0.0024 Least significant bit  
14: + 0.004  
30 13: + 0.010  
12: + 0.020  
11: + 0.040  
10: + 0.078  
9: + 0.156  
35 8: + 0.312  
7: + 0.625  
6: + 1.25

5: + 2.5

4: + 5.0 Most significant bit

The next instruction received is the ACTPS statement. Tester instructions to activate  $V_{CC}$  and  $V_{BB}$  power supplies are generated and then the FRCPN statement is encountered. The first FRCPN command instructs DC setup generator 77 to generate the instructions necessary to set up a digital to analog converter with a 10mA range and a clamping of 2.0v; then to force a value of 800mV on pins P2 and P3. To accomplish this, DC setup generator 77 generates an "A register load" (0A op code) to setup the digital to analog converter to the 10mA range for pin P2. Then a "B register load" (0B op code) is generated to set the digital to analog converter clamp value to the 2.0v range. Then the digital to analog converter is loaded with the 800mV value through the 0D tester op code. These three instructions are then repeated for pin P3. The composition of the value portions of '0B' and '0D' op codes are as follows:

bits 16-27 contain the value  
bits 28-30 contain '010' if 'milli'  
                                  '001' if 'micro'  
bit 31 is '0' if value is in volts  
                                  '1' if value is in amps.

Again, through the use of the footprint file 73, DC Setup Generator 77 converts pins P1, P2, and P3 to tester channels C1, C2, and C3.

The value portion of the '0A' op code is based upon a table where:

if the clamping condition is:                   then the value is:

100 MA	0800
10 MA	0200
1 MA	0100
100 $\mu$ A	0080
10 $\mu$ A	0040
1 $\mu$ A	0020

The second FRCPN statement is processed in a manner similar to that described above. The next statement is the DELAY statement. Op code 91 is the tester op code for delaying processing, the 05 code is the unit of measure in milliseconds and the value of 8 is assigned to the second half-word of the instruction. Finally, the MEAPN statement causes DC setup generator 77 to generate the necessary instructions to measure P1 between a high limit of 500 microamps and a low limit of 100 microamps. Tester op code 93 tells the tester which sort bit to set when a DC fail occurs for this test. In our example, the sort bit is equal to 1. The tester command to load a limit is 0C. The second byte is set to 01 for loading a high limit and is set to 02 for loading a low limit. The next twelve bits are the value setting and the last four bits reflect a unit of measure.

The final tester instruction is the op code to cause the plus side of the digital volt meter to be moved to pin P1 and generate a reading. The op code to do this is 17. When instruction 17C1 is executed by the tester, a reading will be made on pin P1 based on the above forcing conditions to P1, P2 and P3. The tester will compare the reading to the limit specified. If the reading is within the limits, the test was successful. If not, a DC failure will result and the failure will be logged according to the above 93 op code. This completes the description of the translation of the DC Product Test Example universal language instruction sequence into the DC Product Test Example tester instruction sequence (Table 8).

For the DC Test Site example shown in Table 6 expansion of universal language instruction is done in the same manner as for DC test. The TSTID instruction dictates to input manager 67 that this is a DC test. Input manager saves this information and will continuously call DC setup generator 77 until the next TSTID

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instruction is encountered. Table 9 shows the expansion done by DC setup generator 77 on the DC test site example.

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Table 9

DC PRODUCT TEST SITE EXAMPLE

UNIVERSAL LANGUAGE

INSTRUCTION SEQUENCE

DC PRODUCT TEST EXAMPLE

TESTER INSTRUCTION SEQUENCE

5

TSTID DC

{ FF00  
0701 XXXX  
0702 XXXX  
⋮  
0709 XXXX

COMMENT TEST 2

10 DMODE ON

9201

FRCPN -10 $\mu$ A 100 $\mu$ A 10V P1

{ 0AC1 0800  
0BC1 00A0  
0DC1 FF63

15

FRCPN GND 100 $\mu$ A 10V P2,P3

{ 0AC2 0080  
0BC2 00A0  
0DC2 0000  
0AC3 0080  
0BC3 00A0  
0DC3 0000

20 DELAY 80ms

9105 0050

MEAPN B -500MV -700MV 1 P1

{ 9301  
0C01 E0C4  
0C02 D444  
17C1

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Referring now to Table 10, the translation of the AC test universal language source file example of Table 7 into an AC test tester instruction set is illustrated.

AC TEST EXAMPLE UNIVERSAL LANGUAGE  
INSTRUCTION SEQUENCE

Table 10

AC TEST EXAMPLE TESTER  
INSTRUCTION SEQUENCE

5

TSTRID AC

$$\left\{ \begin{array}{l} \text{FF00} \\ 0701 \text{ YYY} \\ 0702 \text{ YYY} \\ \vdots \\ 0709 \text{ YYY} \end{array} \right.$$

COMMENT TEST 3

DIMEN 7 4 6 10 10 2

10

SELPs VCC 0V 1A STANDARD 2V

$$\left\{ \begin{array}{l} 0204 \text{ 0330} \\ 0844 \\ 0404 \text{ 0000} \end{array} \right.$$

$$\left\{ \begin{array}{l} 0202 \text{ 0330} \\ 0842 \\ 0402 \text{ 0CD0} \end{array} \right.$$

15

SELPs VBB -2V 1A STANDARD 2V

$$\left\{ \begin{array}{l} 0201 \text{ 0330} \\ 0841 \\ 0401 \text{ 0800} \end{array} \right.$$

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AC TEST EXAMPLE UNIVERSAL LANGUAGE  
INSTRUCTION SEQUENCE

AC TEST EXAMPLE TESTER  
INSTRUCTION SEQUENCE

ACTPS VCC	0641
ACTPS VBB	0621
5 ACTPS VEE	0611
PGTIM RI 3 20ns 0ns	$\begin{cases} A0RD E800 \\ C0A0 3C00 \end{cases}$
PGTIM W1 3 20ns 0ns	$\begin{cases} A0WT 9800 \\ C020 3C00 \end{cases}$
10 CYCTM 100ns	8500 0064
	2281 0000
	9105 0008
DELAY 8ms	

AC TEST EXAMPLE UNIVERSAL LANGUAGE  
INSTRUCTION SEQUENCE

COMMENT 1 CPC

PATDEL 1

PASDEL 1 1

0701 0001 Preset start register to 1  
0702 0008 Present end of test register  
0703 0001 Preset # of loads required to  
write checkerboard pattern  
8100 Load A & B memories  
0000 0000 0000 Test patterns for write  
0000 0000 0000  
...  
AA00 Execute AC Test (Write  
checkerboard)

PLSPN W1

PASDEL 2 1

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AC TEST EXAMPLE UNIVERSAL LANGUAGE  
INSTRUCTION SEQUENCE

AC TEST EXAMPLE TESTER  
INSTRUCTION SEQUENCE

0701 0001 Preset start register to 1  
0702 0008 Preset end of test register  
8100 Load A & B memories  
0000 0000 0000 Test Patterns for read  
0000 0000 0000  
...  
AA00 Execute AC Test (Read  
checkerboard)

READ 1 1 0 0 3 0 0  
AA00

PLSPN R1

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At the conclusion of expansion of the DC product or test site test, Table 8 or 9, the next statement encountered by input manager 67 is TSTID AC. As with all other universal language source statements, input manager 67 checks this statement against the TSTID value stored. This compare will result in a match, with the operand AC being stored. Then because AC is now stored, input manager 67 links to AC setup generator 74. The TSTID statement causes AC setup generator 74 to generate the tester op code for beginning executing AC testing, i.e., op code FF00. It will be noted that this is the same as the start command for DC testing. Control is then returned to input manager 67 and the COMMENT statement is processed as was described above for the DC Product test (Table 8). Next, input manager 67 encounters the DIMEN statement. Input manager 67 creates a record in file 73 from this statement, according to the format of Table 11. This record is now accessible by AC setup generator and bit pattern generator (74 and 76, respectively).

Table 11

DIMENSION DATA RECORD

Byte #

01	"DIMEN"	Dimension Data i.d.
25	10	# Word Address Lines
	14	# Bit Address Lines
	18	# Control Lines
	22	# Data-In Lines
	26	# Data-Out Lines
30	30	Interwoven/Non-Interwoven

The next six universal language source statements (i.e., three SELPS and three ACTPS instructions in Table 10) contain the same data fields as their DC counterparts. They are processed in the same manner by 5 AC setup generator 74. The next two universal language source statements (i.e., two PGTIM instructions in Table 10) set up timing conditions for read control pin R1 and write control pin W1. Both have a positive, return to zero pulse, and both have a pulse width of 20 10 nanoseconds and a start time at 0 nanoseconds. Each PGTIM instruction causes AC setup generator 74 to generate two tester instructions, the first an A0 and the second a C0. The A0 instruction sets a positive or 15 negative polarity, selects a read or write timing generator from the four available for read control and the four available for write control. Finally, A0 tells the timing generator if the mode is return to zero or non-return to zero. The C0 tester instruction describes a pulse width and start time for the read and 20 write lines. The AC setup generator 74 also uses the footprint file 73 to connect the read control pin R1 to tester channel RD and write control pin W1 to tester channel WT.

The next universal language source statement 25 (Table 10) is CYCTM. This statement sets the tester cycle time for the test. Then, the TEXEC statement is read. This command generates tester instructions to govern AC diagnostic for an upcoming test. AC setup generator 74 generates an op code 22 which according to 30 the TEXEC statement will skip out of the test when the first failure occurs and will log the failure as a 1. Op code data bit 0 will be set to 1 to indicate skip out on first fail while data bits 1-7 will be set to 1 to indicate the class of error and data bits 8-23 will 35 be set to 0 since the mode is stop on first fail. The next statement encountered is the DELAY statement. AC setup generator 74 processes this statement the same as

DC setup generator 77. The COMMENT statement will be handled in the same manner as for DC setup (Table 8).

The PATDEL statement is the first command encountered which causes AC setup generator 74 to forward 5 control to bit pattern generator 76. Bit pattern generator 76 extracts the information it needs from the PATDEL statement. Then, bit pattern generator 76 receives the PASDEL statement. This tells bit pattern generator 76 that this is pass number 1 and that there 10 will be 1 read/write operation per array cell. The PATDEL and PASDEL statements do not cause any op codes to be generated. Their purpose is to pass necessary bit pattern generation information to the bit pattern generator. The last piece of information which bit 15 pattern generator needs prior to generating the required bit pattern is the WRITE statement. The WRITE statement specifies that addressing will be in the word direction and that it will be incremental. The WRITE statement also tells bit pattern generator 76 that the 20 start value is zero. This statement data together with the array dimension data on file is all the information which bit pattern generator 76 needs to generate the test pattern.

The information required to generate the 1 cycle 25 per cell bit pattern is derived by bit pattern generator 80 as follows: The size of the array is derived from the number of word addresses, bit addresses, and the number of data lines. In the present example, the size is 128x16x10 or 20K, derived from the seven word 30 address lines, four bit address lines and ten data lines. The WRITE statement also specifies that addressing priority should be in the word direction which means that the word lines all must change before the bit address line changes. The WRITE statement also 35 provides the addressing direction which in this particular example is incremental. This means that processing begins at word address =0 and bit address=0 as

opposed to word address=127 bit address=15. The WRITE statement also conveys the information that the writing into the array is in a checkerboard pattern beginning with the value 0. Fig. 10 illustrates the above described derivation of the bit pattern generation data for the memory array of the present example.

Prior to describing generation of the bit pattern of the present example by bit pattern generator 76, a more detailed description of the tester memory 84 (Fig. 9) will be presented. For this particular example, it will be assumed that the tester memory 84 includes two data matrices with a total of 18,432 bits. Each data matrix is organized as a 36 bit by 256 word array. The data matrices will be referred to as the A and B memories. The 36 bit dimension of the A and B memory comprises data bits, address bits and control bits. There are several modes of operation available. For the present example, it is assumed that the A memory cycles sequentially between the value contained in a start register and the value programmed using the A memory control bits. Memory transitions occur at each clock cycle. The B memory cycles sequentially between words 0 and 255. The time of change in B memory from a word to the next sequential word is controlled by the A memory program control field. The control field bits of the A and B memory are as follows: The A control bits comprise an increment B bit (INC B), an A branch bit (BRN) and an end of program marker (PTR). The INC B bit tells the tester when to increment to the next word in the B memory. The BRN bit signals the tester to branch to the A memory address specified in the start register, and the PTR bit marker instructs the tester that the end of the program has been reached or that a reload of the start register may be performed.

The B memory control bits comprise a store command bit (STR), a select command bit (SEL), and a pass-through bit (PAS). The STR bit specifies the A memory

address to be stored into the start register. The SEL bit works with the BRN command to specify the start register S1 or S2. It also operates with STR to specify S1 or S2. For the checkerboard example being 5 described here, only 1 start register is required to be programmed. For other bit pattern applications two start registers must be employed in the programming. The PAS bit is programmed similar to BRN. The A memory address passed to is two greater than the one which 10 appears simultaneously with PAS=1. Instruction timing occurs on every second clock cycle. Table 12 illustrates the complete layout of the A and B memories.

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Table 12  
A and B Memory Formats

A-Memory (36 bits x 256 words)

	<u>Bits</u>	<u>Purpose</u>
5	1-22	data bits 1-10 used; 1 for each data line 11-22 unused
	23-30	unused
	31-36	control bits
10		31 Block (do not allow) write 32 Block (do not allow) read 33 cycle 34 INC-B 35 BRN-A
15		36 PTR

B-Memory (36 bits x 256 words)

	<u>Bits</u>	<u>Purpose</u>
	1-21	data bits - unused
	22	cycle trip
20	23-33	address bits 23-29 word bit address lines 30-33 bit address lines
	34-36	control bits 34 STR 35 SEL 36 PAS
25		

Fig. 11 illustrates a shorthand simulated version of the checkerboard bit patterns generated by bit pattern generator 76 (Fig. 8). By this it is meant that A memory will contain words 0, 1, 2, .... 3, 2 and not 0, 1, 2, 1, 2, .... 31, 32, 31, 32. Fig. 11 illustrates memory addresses 0-4, however, it will be understood by those having skill in the art, that to fully write the array with a checkerboard pattern requires 32 A memory words and 256 B memory words. To read the entire checkerboard pattern requires an additional 32 words of A memory.

After creating the bit patterns, bit pattern generator 76 writes the bit patterns into the Notes file 75. This is done in anticipation of future bit pattern requirements in the same AC test which may require the same A memory and/or B memory patterns. This is probable when the same patterns are required for several different voltage or timing cases. When this occurs, bit patterns can be retrieved and repeated rather than being regenerated each time.

Referring again to Fig. 11, the contents of the A and B memory and the manner in which checkerboard bit patterns are generated from these memories by tester 21 will be described. The cycle bit of the A and B memories determine how many times the tester must cycle through the A and B memory. Whenever the cycle bits of the A and B memories match, two things will occur. First, the preset number of cycles register is reduced by 1. When this register count becomes zero, the tester will stop processing bit patterns and process the next tester op code. Second, the array addressing is incremented as programmed. In this example, the bit direction address is increased. For this checkerboard example, the A and B memory cycle bits will match at B memory addresses 0 and 128. The tester circuitry is set up in such a way as to ignore the first occurrence or the first matching condition. Therefore, the

checkerboard patterns will be applied first to word addresses 0-127, bit address 0. At word 128, the next match occurs. This causes the word address line to reset to 0 and the bit address lines to be increased by 5 1. Thus, there will be a complete cycle through the word addresses for each bit address. To write through the entire array will require eight matches. This is an essential piece of information to the tester, because it communicates the number of times the tester 10 must cycle through B memory in order to complete the writing into the array. This data (end-of-test) is sent to AC setup generator 74 which then writes out to the AC setup 79 file the necessary tester instructions (see Table 10) so that end of test can be properly 15 sensed. To complete the checkerboard write and read, 16 matches are required. Fig. 11 represents the subset of the patterns necessary to perform the write portion of the test. This is reflected in the settings of the block write/read bits; i.e., the block write bit is 0 20 and the block read bit is 1 indicating write only. To write a checkerboard pattern into the 128x16x10 array of our example, will only require one load, i.e.,  $\leq 256$  A memory or B memory words. The number of loads required to perform the WRITE is communicated to AC 25 setup generator 74 which generates the appropriate tester instructions (see Table 10) and writes the instructions into AC setup file 79.

The tester instructions to load the A memory and B memory are next. First bit pattern generator 76 checks 30 to determine if this set of bit patterns has been written to the Notes file 75. It determines that these patterns are not as yet on the Notes file so bit pattern generator 76 writes these patterns to the Notes file. Next bit pattern generator 76 communicates to AC 35 setup generator 74 to write the patterns to AC setup file 79. Bit pattern generator 76 tells AC setup generator 74 where the proper bit patterns are located

on the Notes file. AC setup generator 74 then writes out a load command (op code 81, Table 10) and the bit patterns from the Notes file (see Table 10). All writing of bit patterns will be done in the same 5 manner: bit pattern generator 76 will either generate the patterns and write them to Notes file or find them already in Notes file. In either case, bit pattern generator 76 will return to AC setup generator 74 with instructions to issue a load command and with a pointer 10 to the Notes file for the proper patterns to load.

Control is now returned to the input manager 67 (Fig. 8). The next statement (Table 10) is processed. It is the PLSPN statement. This statement will actually cause tester execution of the write bit patterns 15 already loaded into A and B memories. PLSPN is sent to AC setup generator 74 for translation. AC setup generator 74 converts PLSPN to the op code AA which means execute AC testing. Finally, processing of the remaining PASDEL, READ and PLSPN commands of Table 10 20 are the same as for the write pass described above with regard to Table 10 because the READ operation requires the same patterns as the WRITE except for the "block read" and "block write" settings in A memory. The start register and the end of processing registers must 25 also be reset. Table 10 details these operations for the READ statement.

Thereafter, control is returned to input manager 67 (Fig. 8) which determines that there are no more commands to process. Input manager 67 then passes 30 control to output manager 82 with parameters indicating that both DC and AC test data has been generated. Output manager 82 simply concatenates the DC and AC test into a single tester instruction sequence 30X. At the end of each DC and AC test an ENDTEST instruction 35 is inserted by output manager 82 to indicate that the tester should stop processing instructions.

CLAIMS

1. A system for automatically testing an integrated circuit memory array (25A...25X) on one of a plurality of different array testers (21A...21X), characterized by:
  - 5 a data entry device (12) for entering therein tester independent test specifications (20A...20N) for said array;
  - 10 a universal language generator (14) for generating a tester independent universal language instruction sequence (16) for carrying out prescribed tests for said array, based upon the entered test specifications; and
  - 15 a plurality of universal to tester translators (19A...19X), each of which is associated with a respective one of said plurality of different array testers, for translating said tester independent universal language instruction sequence into a tester dependent instruction sequence (30A...30X) for carrying out said prescribed tests for said array on the associated tester.
2. The system of claim 1, characterized in that said data entry device (12) is an interactive data entry device.
- 25 3. The system of claim 1, characterized in that said tester independent test specifications (20A...20N) comprise characterizing information, DC testing parameters, AC testing parameters and AC test pattern choices for said array, and that said prescribed tests comprise DC parametric tests, AC parametric tests and AC pattern tests for said array.

4. The system of claim 2, further characterized by a data entry manager (11) for controlling the interactive entry of said tester independent test specifications (20A ...20N) on said interactive data entry device (12).

5 5. The system of claim 1, further characterized by a universal to tester translator selector (18) for routing said tester independent universal language instruction sequence (16) to the appropriate one of said plurality of universal to tester translators (19A...19X).

10 6. The system of claim 3, characterized in that said universal language generator (14) comprises a universal language generator controller (36) for accepting the entered tester independent characterizing information, DC testing parameters, AC testing parameters and AC 15 test pattern choices; a DC universal language generator (37) for generating the universal language instruction sequence for carrying out said DC parametric tests; and an AC universal language generator (38) for generating the universal language instruction sequence for carrying 20 out said AC parametric tests and AC pattern tests.

7. The system of claim 3, characterized in that each of said universal to tester translators (19A...19X) includes an input manager (67) for accepting the tester independent universal language instruction sequence; a DC 25 setup generator (77) for generating the tester dependent instruction sequence for carrying out said DC parametric tests; an AC setup generator (74) for generating the tester dependent instruction sequence for carrying out said AC parametric tests; and a bit pattern generator 30 (76) for generating the tester dependent instruction sequence for carrying out said AC pattern tests.

8. The system of claim 4, characterized in that said data entry manager (11) audits the entered tester independent test specifications (20A...20N) for completeness and consistency.

5 9. A method of automatically testing arrays (25A...25X) of varying configurations on array testers (21A...21X) of varying designs, characterized by operating one or more computers to carry out the steps of:  
10 providing means for entering tester independent test specifications (20A...20N) for an array to be tested;  
generating a tester independent universal language instruction sequence (16) based upon the entered test specifications;  
15 translating said tester independent universal language instruction sequence into a tester dependent instruction sequence (30A...30X) which is compatible with the particular array tester (21A...21X) to be employed; and,  
20 applying said tester dependent instruction sequence to the particular array tester to be employed, to thereby test said array thereon.

25 10. The method of claim 9, characterized in that said providing step comprises the step of presenting menus (Fig. 3A...3L) on a data entry device (12) for entry therein of tester independent test specifications (20A...20N) for an array (25A...25X) to be tested.

30 11. The method of claim 9, characterized in that said tester independent test specifications (20A...20N) comprise characterizing information, DC testing parameters, AC testing parameters and AC test pattern choices for said array.

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12. The method of claim 9, characterized in that the following step is carried out between said providing step and said generating step:

5 auditing the tester independent test specifications (20A...20N) for completeness and consistency.

13. The method of claim 9, characterized in that said applying step comprises the step of loading said tester dependent instruction sequence (30A...30X) into the tester memory of the particular array tester

10 (21A...21X) to be employed.

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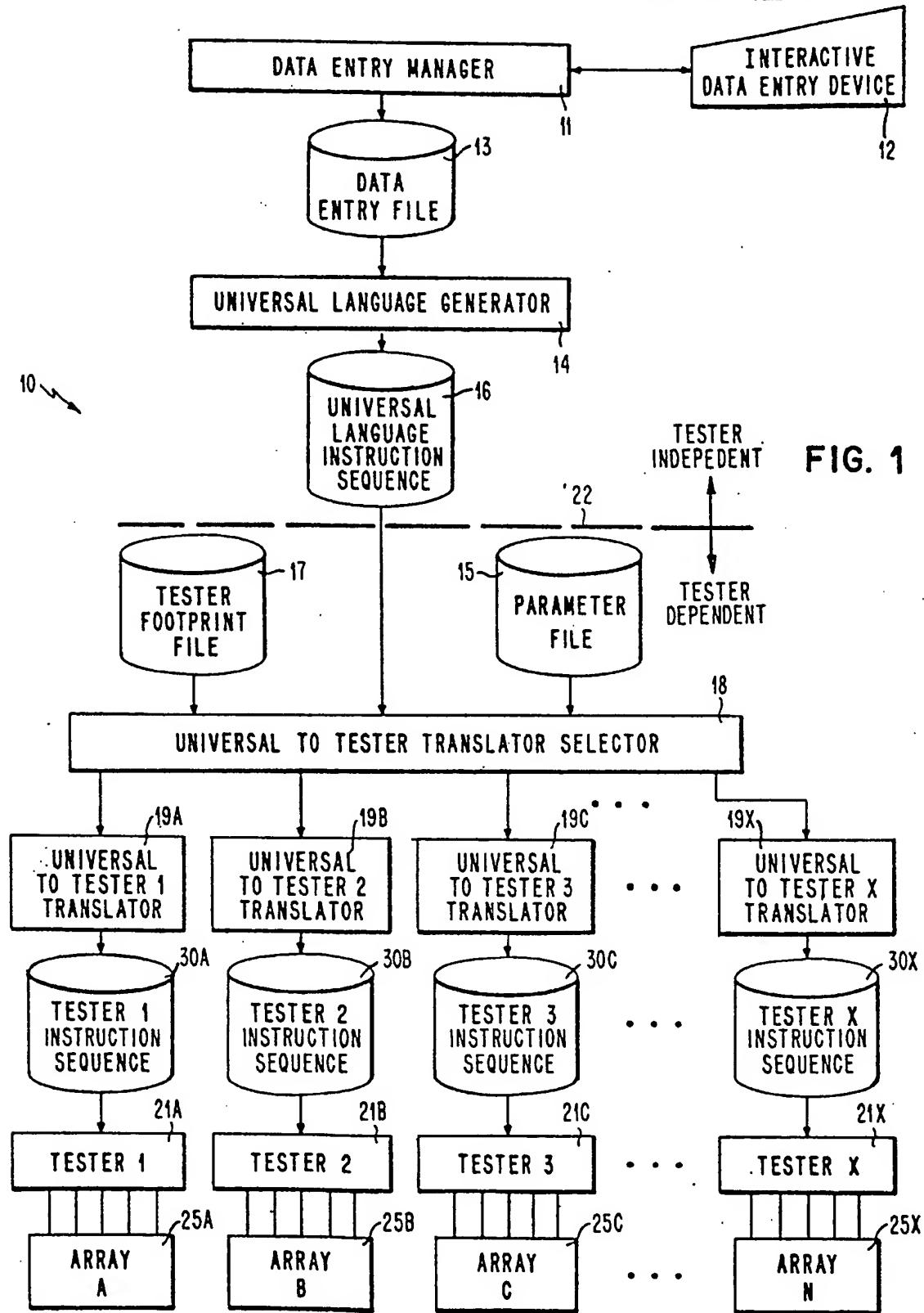
 20A, 20B, 20C, 20N,  
 SPEC A SPEC B SPEC C ... SPEC N


FIG. 1

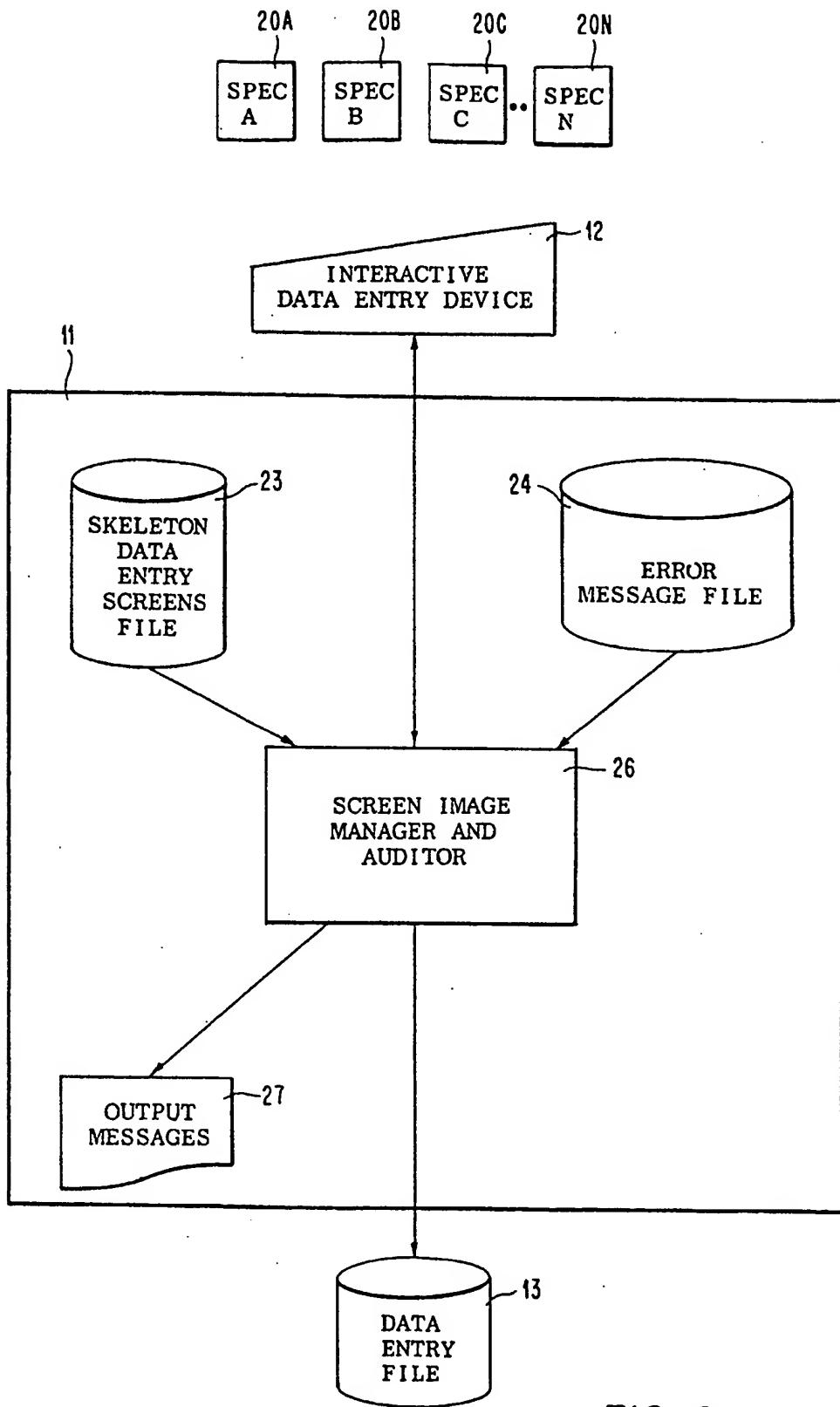


FIG. 2

PRIMARY OPTION MENU SCREEN

## SELECT OPTION \_\_\_\_\_

- (1) DC ARRAY LIBRARY ALLOCATIONS (MUST BE SELECTED 1ST FOR DC)
- (2) AC ARRAY LIBRARY ALLOCATIONS (MUST BE SELECTED 1ST FOR AC)
- (3) DC TEST DATA ENTRY (SUPPLY AND TEST CONDITIONS)
- (4) AC TEST DATA ENTRY (SUPPLY AND TEST CONDITIONS)
- (5) FOREGROUND PROCESSING (ON LINE AUDITOR)
- (6) BACKGROUND PROCESSING

FIG. 3A

DC ARRAY LIBRARY ALLOCATION SCREEN

## ENTER PARAMETERS BELOW:

TECHNOLOGY	→	(3 CHARACTERS)
PRODUCT TYPE	→	( <u>WAFER</u> , <u>MODULE</u> , <u>TESTSITE</u> )
PART # ID	→	(8 CHARACTERS)
ENGINEERING CHANGE LEVEL	→	(8 CHARACTERS)
DISPOSITION	→	( <u>NEW</u> , <u>MOD</u> , OR <u>OLD</u> )

FIG. 3B

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AC ARRAY LIBRARY ALLOCATIONS SCREEN

ENTER PARAMETERS BELOW:

TECHNOLOGY → \_\_\_\_\_ (3 CHARACTERS)  
PRODUCT TYPE → \_\_\_\_\_ (WAFER, MODULE)  
  
PART NUMBER → \_\_\_\_\_  
ENGINEERING CHANGE LEVEL → \_\_\_\_\_  
# OF WORD ADDRESSES → \_\_\_\_\_  
# OF BIT ADDRESSES → \_\_\_\_\_  
# OF DATA LINES → \_\_\_\_\_  
# OF CONTROL LINES → \_\_\_\_\_  
DESIGN → \_\_\_\_\_ (INTERWOVEN OR NON  
INTERWOVEN)  
DISPOSITION → \_\_\_\_\_ (NEW, MOD, OR OLD)

FIG. 3C

DC TEST DATA ENTRY SCREEN

PROJECT → \_\_\_\_\_ (6 CHARACTER USER IDENTIFICATION)  
LIBRARY → \_\_\_\_\_ (TEST PROGRAM NAME, SEE BELOW)  
MEMBER → \_\_\_\_\_ (BLANK FOR SELECTION LIST)

## TEST PROGRAM NAME GENERATION:

THE TEST PROGRAM NAME IS GENERATED BY SUBSTITUTING THE FOLLOWING

XXX - TECHNOLOGY  
Z - FIRST LETTER OF PRODUCT TYPE  
S - EC SUFFIX LEVEL

FIG. 3D

SUPPLY MENU SCREEN

TOTAL # OF POWER SUPPLY CASES \_\_\_\_\_ (2 DIGITS)

POWER SUPPLY CASE # \_\_\_\_\_ (2 DIGITS)

V/I CARD:	→	$V_{CC}$	$V_{BB}$	$V_{EE}$	$V_{11}$	$V_{22}$
GROUP 1	→					
GROUP 2	→					
PSCLAMP	→	2V	-2V	-2V		
PS RANGE	→	1A	1A	1A		
MODE		STANDARD	STANDARD	STANDARD		

NOTE: MODE = STANDARD, DUAL OR MULTIPLE)

## I/O DEFAULTS:

I/O CLAMP → 10V

I/O RANGE → 10MA (10 $\mu$ A, 100 $\mu$ A, 1MA, 10MA, 100MA)

FIG. 3E

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DC TEST LIMITS SCREEN

TEST NAME	→	MEASURED PIN	→		
DIAGNOSTIC #	→	01	HIGH LIMIT	→	
DELAY	→		LOW LIMIT	→	
POWER SUPPLY CASE # →					
PIN	VALUE	PIN	VALUE	PIN	VALUE
→	→	→	→	→	→
→	→	→	→	→	→
→	→	→	→	→	→
→	→	→	→	→	→
→	→	→	→	→	→
→	→	→	→	→	→
→	→	→	→	→	→
→	→	→	→	→	→
→	→	→	→	→	→
→	→	→	→	→	→
IF WRITE REQUIRED:					
TYPE	→	(AC OR DC)	LEAD	→	
PIN	→		TRAIL	→	
RETURN TO ZERO	→	(YES, NO)	→		

FIG. 3F

DC TEST SITE LIMITS MENU SCREEN

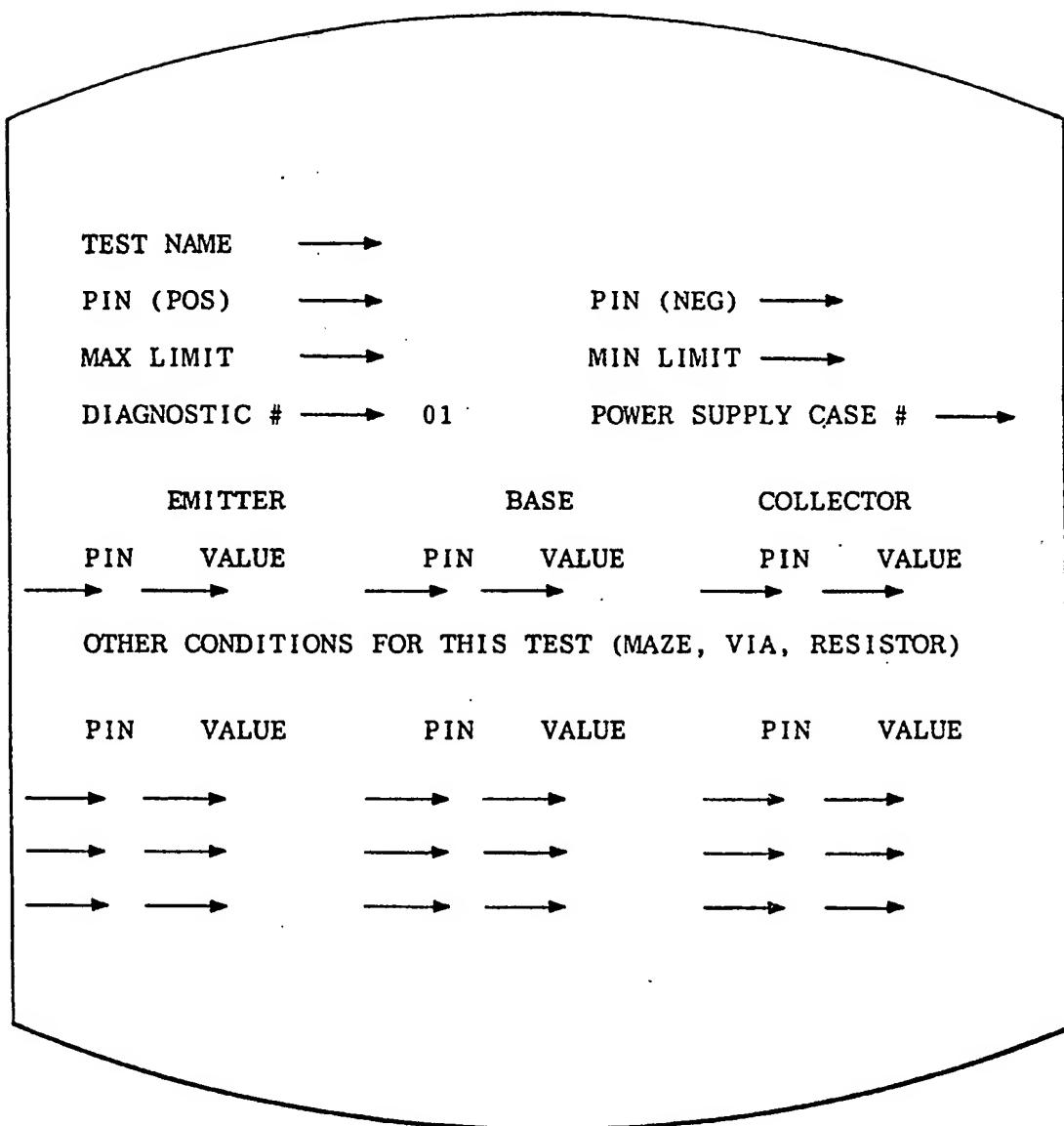


FIG. 3G

AC TEST DATA ENTRY SCREEN

PROJECT → (6 CHARACTER USER IDENTIFICATION)  
LIBRARY → (TEST PROGRAM NAME, SEE BELOW)  
MEMBER → (BLANK FOR SELECTION LIST)

## TEST PROGRAM NAME GENERATION:

THE TEST PROGRAM NAME IS GENERATED BY SUBSTITUTING THE FOLLOWING

XXX - TECHNOLOGY  
Z - FIRST LETTER OF PRODUCT TYPE  
S - EC SUFFIX LEVEL

FIG. 3H

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AC TEST LIMITS SCREEN

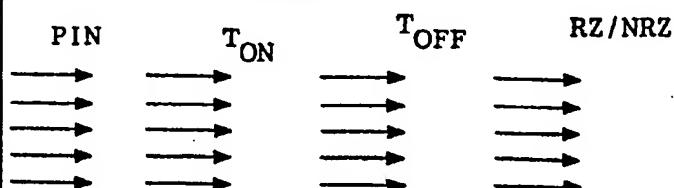
TEST NAME →

POWER SUPPLY CASE # →

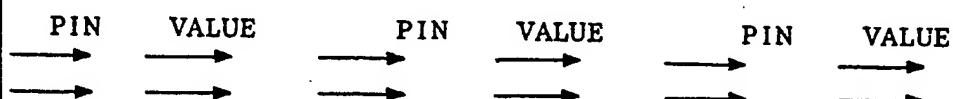
DIAGNOSTIC # → 01

CYCLE TIME →

PIN TIMINGS:



POWER/INPUT/OUTPUT PINS:



PATTERNS:

PATTERN GROUP → (1 CYCLE/CELL)

TOTAL PASSES →

PASS # →

CMODE → (INCREMENT, DECREMENT)

CADDRESS DIRECTION → (RIPWORD, RIPBIT ....)

HMODE → (INCREMENT, DECREMENT)

HADDRESS DIRECTION → (RIPWORD, RIPBIT ....)

N2 SKIP WORD → N2 SKIP BIT →

PULSE:

PIN 1 → PIN 2 → PIN 3 → PIN 4 → PIN 5 →

FUNCTION:



FIG. 3I

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ADDITIONAL PASS SCREEN

PASS #



CMODE



(INCREMENT, DECREMENT)

CADDRESS DIRECTION



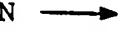
(RIPWORD, RIPBIT)

HMODE



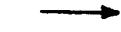
(INCREMENT, DECREMENT)

HADDRESS DIRECTION



(RIPWORD, RIPBIT)

N2 SKIP WORD



N2 SKIP BIT

PULSE:

PIN 1

PIN 2

PIN 3

PIN 4

PIN 5

FUNCTION:



FIG. 3J

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FOREGROUND PROCESSING SCREEN

SCREEN IMAGE ENTRY SOURCE

PROJECT → (6 CHARACTER USER IDENTIFICATION)  
LIBRARY → (TEST PROGRAM NAME, SEE BELOW)

TEST PROGRAM NAME GENERATION:

THE TEST PROGRAM NAME IS GENERATED BY SUBSTITUTING THE FOLLOWING:

XXX - TECHNOLOGY

Z - FIRST LETTER OF PRODUCT TYPE

S - EC SUFFIX LEVEL

FIG. 3K

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BACKGROUND PROCESSING SCREEN

SCREEN IMAGE ENTRY SOURCE

PROJECT → (6 CHARACTER, USER IDENTIFICATION)  
LIBRARY → (TEST PROGRAM NAME, SEE BELOW)

OPTIONS:

DC UNIVERSAL LANGUAGE GENERATION → (YES/NO)  
AC UNIVERSAL LANGUAGE GENERATION → (YES/NO)  
TESTER →  
DC TEST INSTRUCTION SET → (YES/NO)  
AC TEST INSTRUCTION SET → (YES/NO)

TEST PROGRAM NAME GENERATION:

THE TEST PROGRAM NAME IS GENERATED BY SUBSTITUTING THE FOLLOWING:

XXXX - TECHNOLOGY

Z - FIRST LETTER OF PRODUCT TYPE

S - EC SUFFIX

FIG. 3L

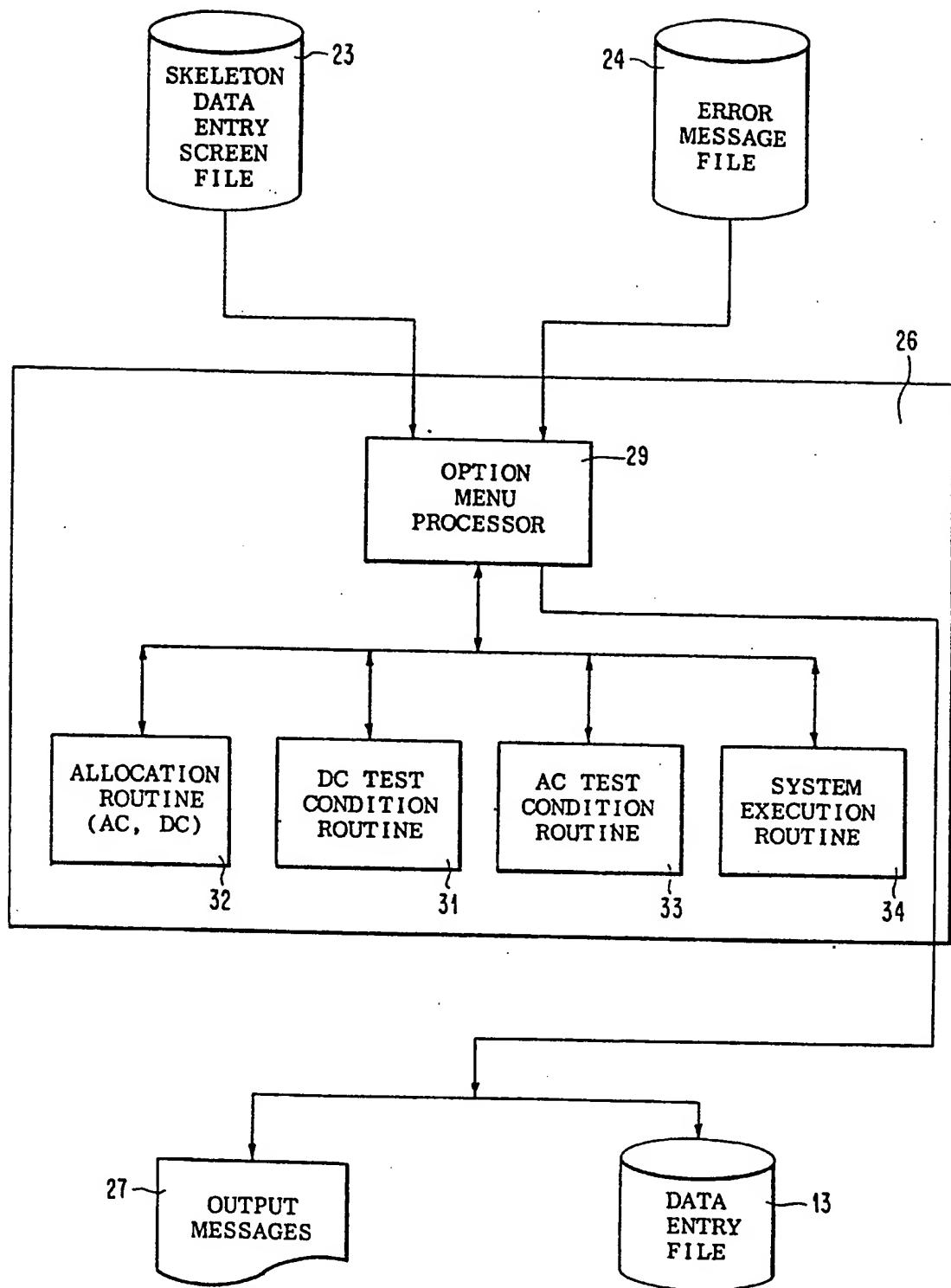


FIG. 4

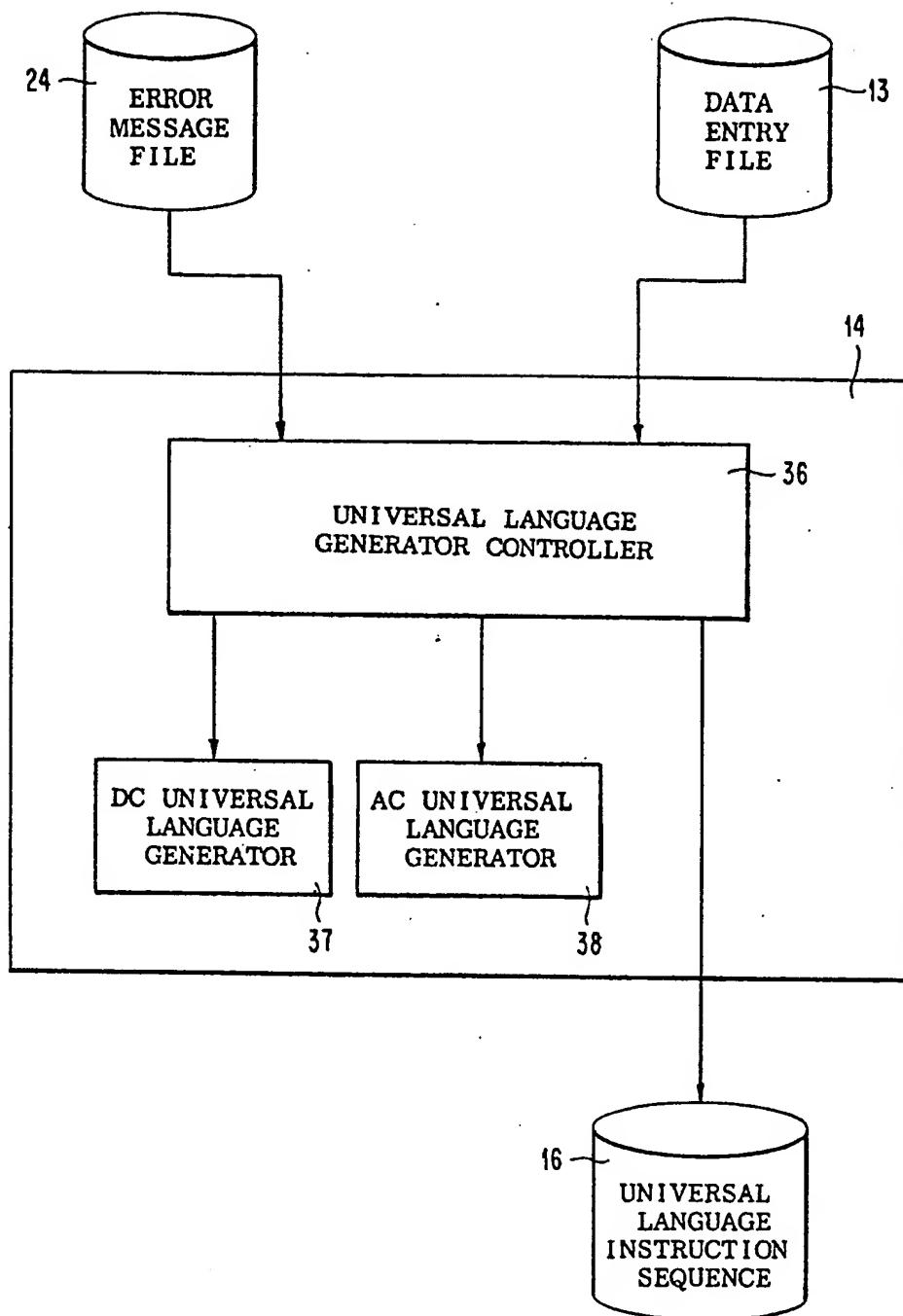


FIG. 5

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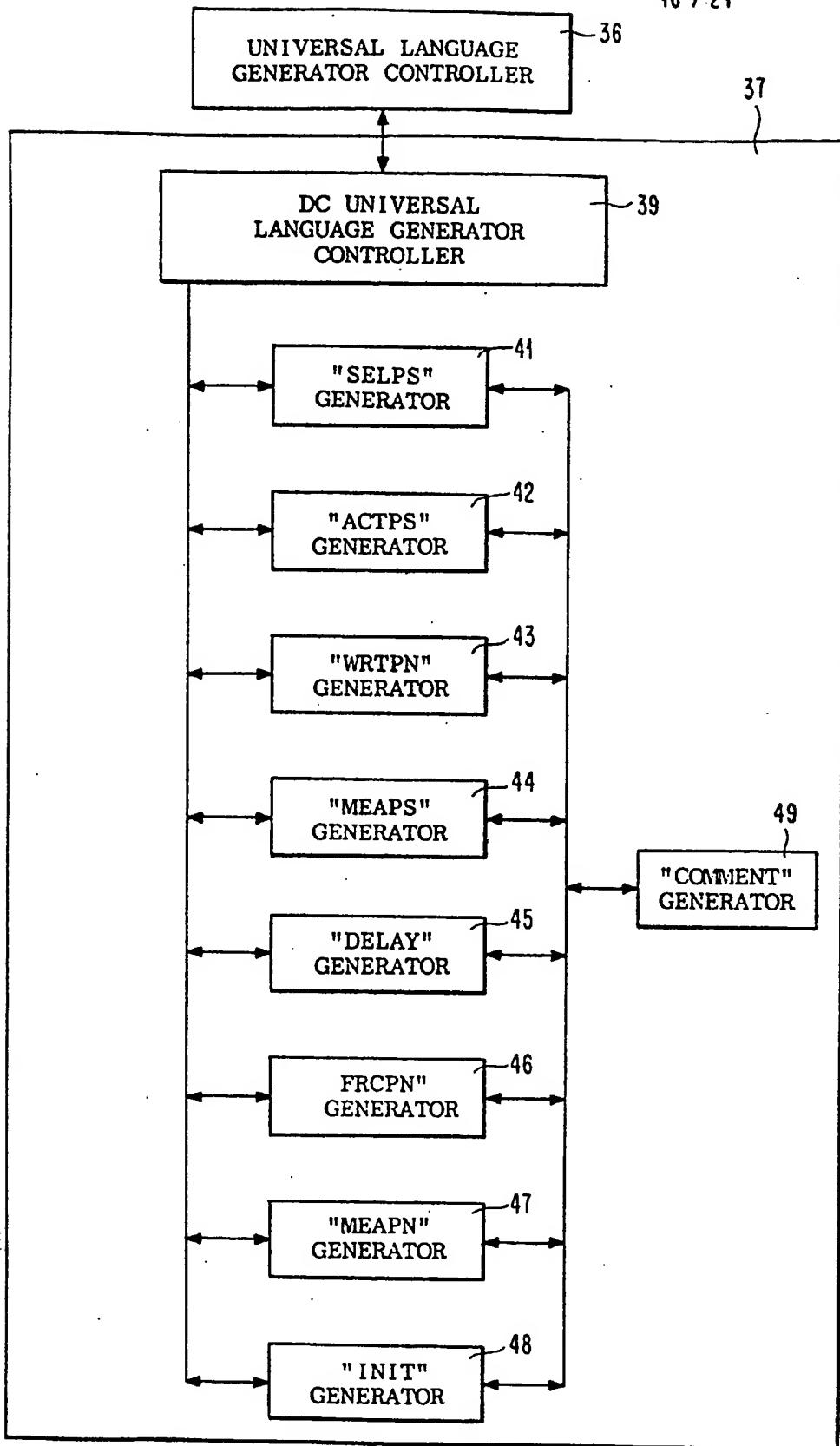


FIG. 6

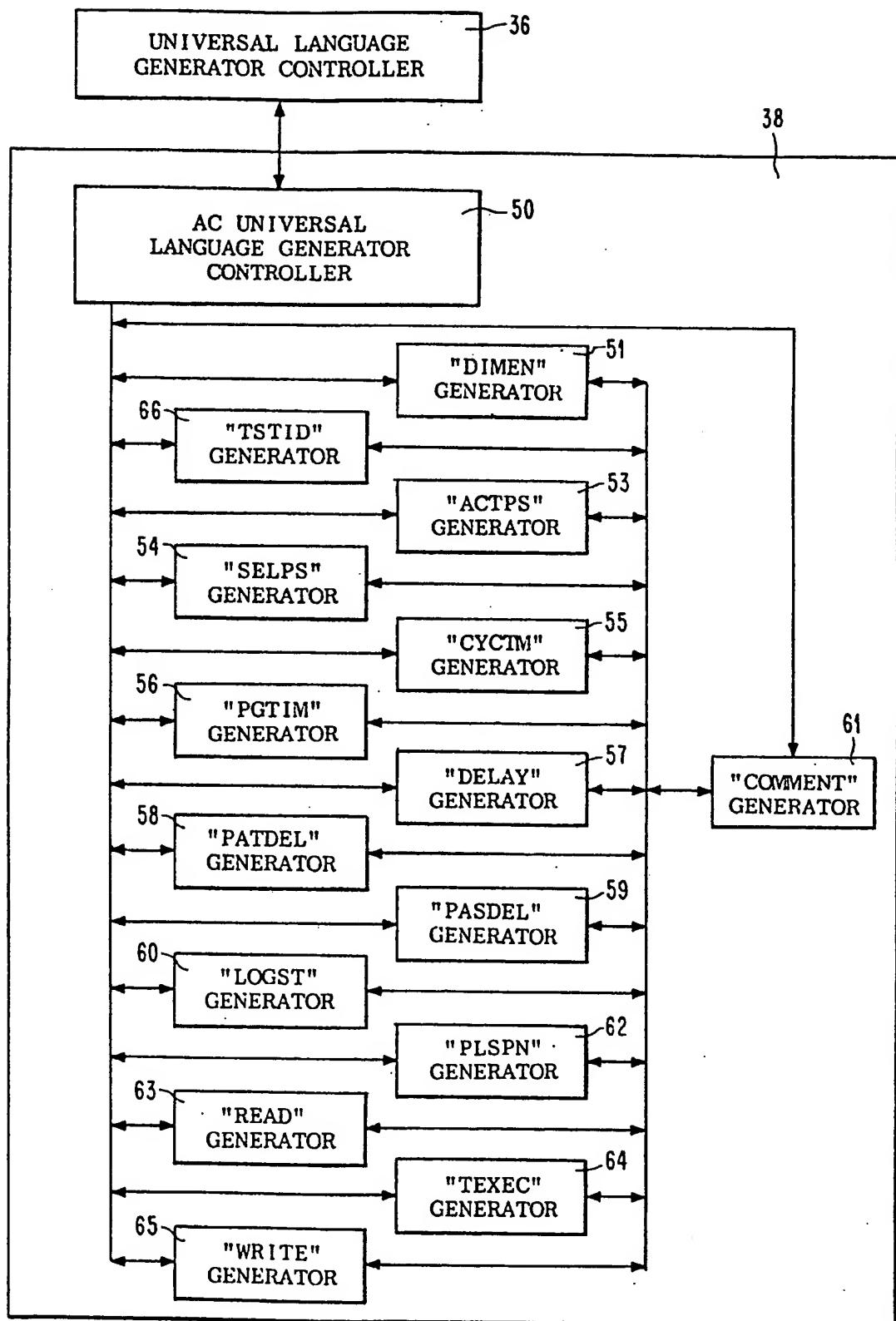


FIG. 7

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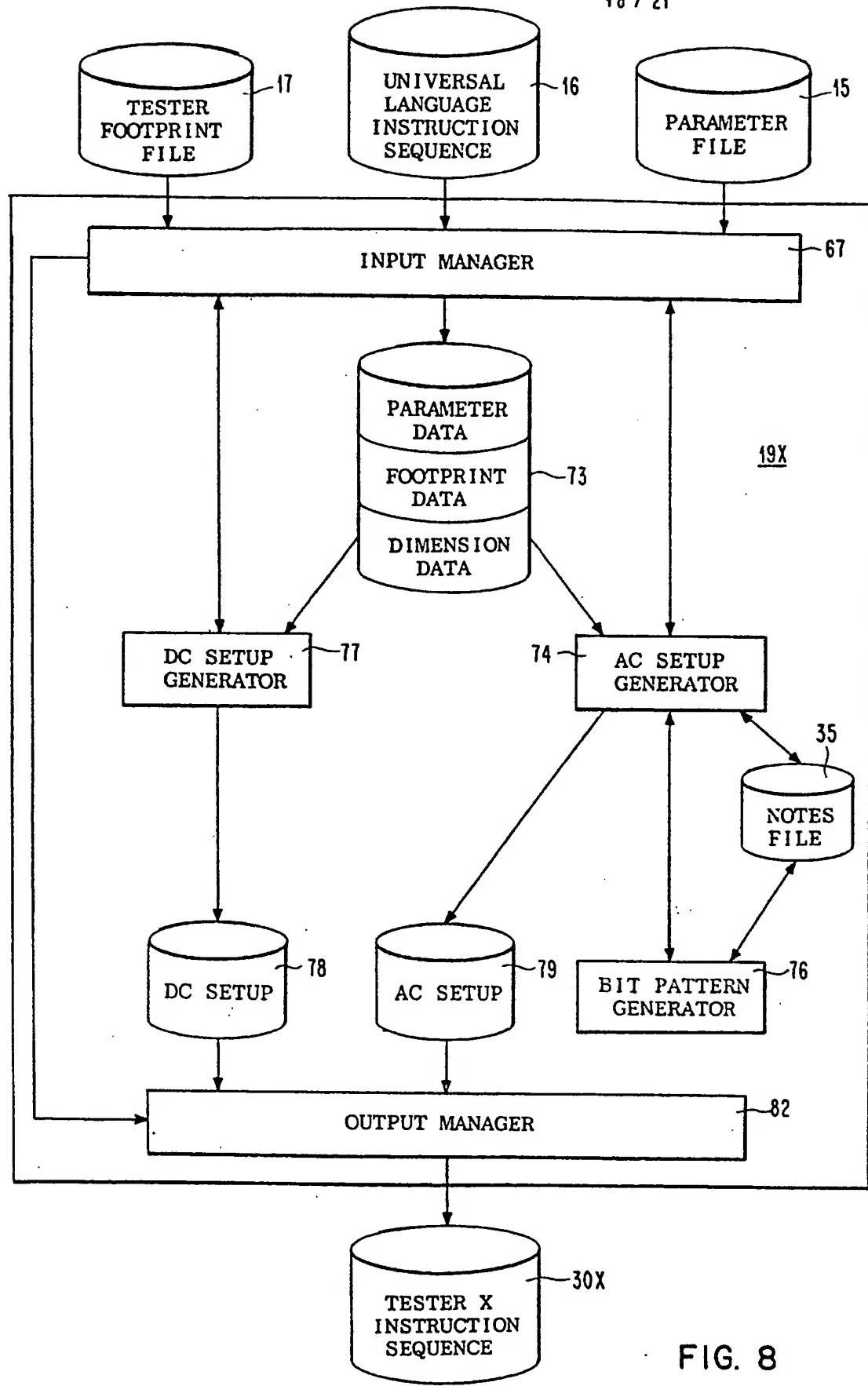


FIG. 8

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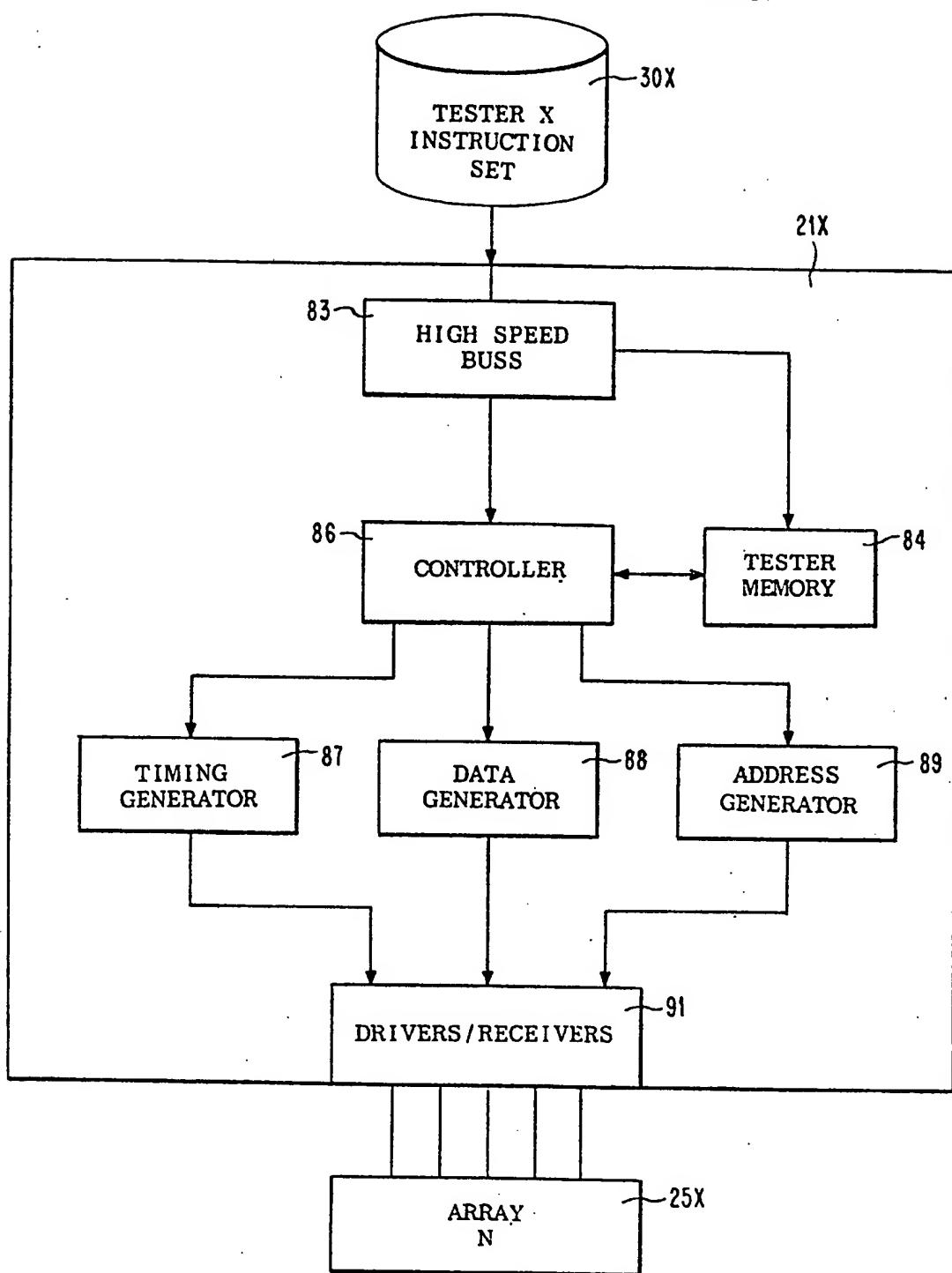
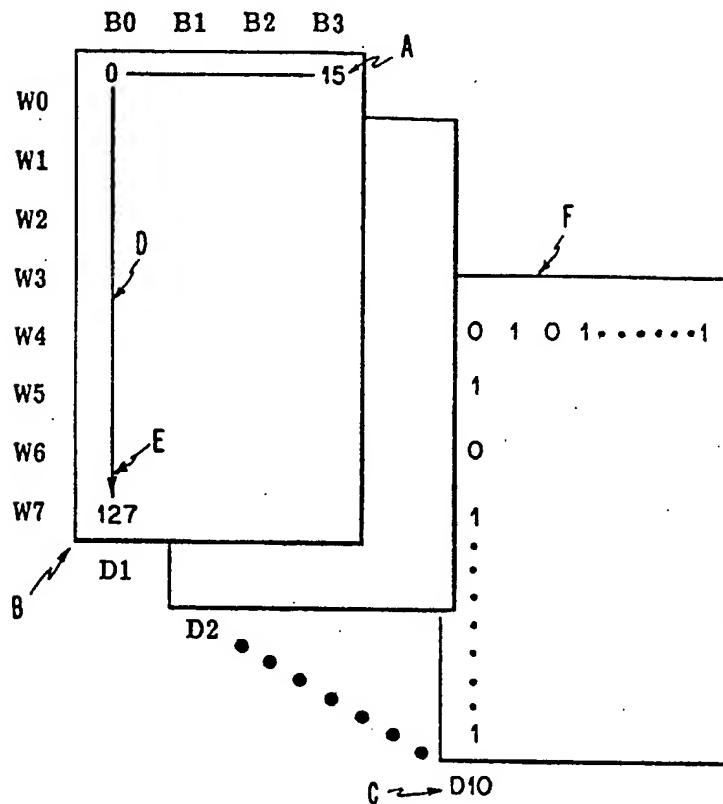


FIG. 9

BIT PATTERN GENERATION DATAInformation

- A - NUMBER OF BIT ADDRESS LINES ( 4 )
- B - NUMBER OF WORD ADDRESS LINES ( 7 )
- C - NUMBER OF DATA LINES ( 10 )
- D - ADDRESSING PRIORITY (WORD)
- E - ADDRESSING DIRECTION (INCREMENTAL)
- F - TYPE OF PATTERN (CHECKERBOARD - 0 )

Origin

- DIMEN: AC UNIVERSAL LANGUAGE STATEMENT (TABLE 4)
- DIMEN: AC UNIVERSAL LANGUAGE STATEMENT (TABLE 4)
- DIMEN: AC UNIVERSAL LANGUAGE STATEMENT (TABLE 4)
- WRITE: AC UNIVERSAL LANGUAGE STATEMENT (TABLE 4)
- WRITE: AC UNIVERSAL LANGUAGE STATEMENT (TABLE 4)
- WRITE: AC UNIVERSAL LANGUAGE STATEMENT (TABLE 4)

FIG. 10

## CHECKERBOARD BIT PATTERNS

WORD #	A-MEMORY		B-MEMORY		A-MEMORY		B-MEMORY		A-MEMORY		B-MEMORY	
	WORD	DATA BITS	BLOCK	YINC	BRNA	PTR	CYCLE	WORD	BIT LINES	WORD	BIT LINES	WORD
#	1-10							0-6	0-3	#	0-3	
0	0-0	1	1	1	1	0	1	00000000	00000	0	0	DUMMY
1	0-0	0	0	1	1	1	0	00000001	00000	0	0	(0,0)
2	1-1	0	0	1	1	0	0	00000010	00000	0	0	(1,0)
1	0-0	0	0	1	1	0	0	00000011	00000	0	0	(2,0)
2	1-1	0	0	1	1	0	0	00000011	00000	0	0	(3,0)
3	1-1	0	0	1	1	0	0	11111110	00000	1	0	126 (126,0)
1	0-0	0	0	1	1	0	0	11111111	00001	0	0	127 (127,0)
2	1-1	0	0	1	1	0	0	00000000	00001	0	0	128 (0,1)
3	1-1	0	0	1	1	0	0	00000001	00000	0	0	129 (1,1)
4	0-0	0	0	1	1	0	0	00000010	00000	0	0	130 (2,1)
3	1-1	0	0	1	1	0	0	00000011	00000	0	0	131 (3,1)
4	0-0	0	0	1	1	0	0	11111110	00001	1	0	254 (126,1)
3	1-1	0	0	1	1	0	0	11111111	00001	0	0	255 (127,1)
4	0-0	0	0	1	1	0	0	11111111	00001	0	0	
8	0-0	0	1	0	0	0	0	11111111	00111	0	0	255 (127,3)
12	0-0	0	1	0	0	0	0	0101	0101	0	0	(127,5)
16	0-0	0	1	0	0	0	0	0111	0111	0	0	(127,7)
20	0-0	0	1	0	0	0	0	1001	1001	0	0	(127,9)
24	0-0	0	1	0	0	0	0	1011	1011	0	0	(127,11)
28	0-0	0	1	0	0	0	0	1101	1101	0	0	(127,13)
32	0-0	0	1	0	0	0	0	1111	1111	0	0	(127,15)

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FIG. 11